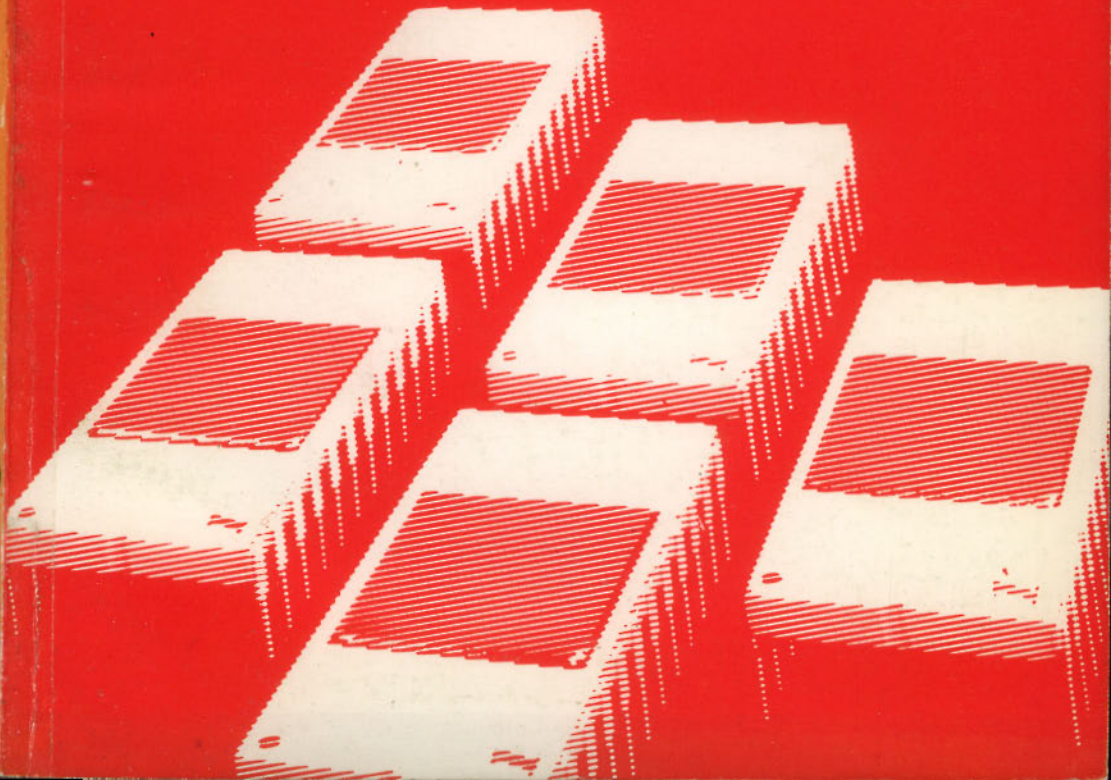
APRIL 1984

TELECOMMS INTEGRATED CIRCUIT HANDBOOK

PLESSEY
Semiconductors



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PLESSEY
Semiconductors

TELECOMMS INTEGRATED CIRCUIT HANDBOOK

Designed and produced by Peter Wigens Consultants
Cover design by Roles and Parker Ltd.

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Contents

Product index

N-Channel MOS

CMOS

CMOS (continued)

Bipolar

Selection guide

		EQUIVALENT	PAGE
N-CHANNEL MOS DATA COMMUNICATIONS CIRCUITS			
MJ2812	32 x 8-bit FIFO memory	AM2812	63
MJ2813	32 x 9-bit FIFO memory	AM2813	63
MJ2841	64 x 4-bit FIFO memory	AM2841	69
N-CHANNEL MOS PCM CIRCUITS			
MJ1410	8-bit format converter		17
MJ1440	HDB3 encoder/decoder		23
MJ1444	Time slot zero transmitter		29
MJ1445	Time slot zero receiver		33
MJ1446	Time slot access		37
MJ1471	AM1/HDB3 encoder/decoder	CD22103	41
MJ1472	PCM receiving circuit		47
MJ1473	PCM transmitter circuit		51
MJ1474	PCM elastic store		55
			59
MODULATORS			
SL1001A	1MHz modulator		159
SL1496C	20MHz double-balanced modulator/ demodulator (commercial)	MC1496G/L/P	167
SL1596C	20MHz double-balanced modulator/ demodulator (MIL)	MC159G/L	167
TELEPHONE COMMUNICATIONS CIRCUITS			
SL1021A	+10dBm channel amplifier		163
SL1021B	+13dBm channel amplifier		163
SL8204	Tone ringer		171
SP1450B	34 Mbit/s PCM signal monitor		177
SP1450B(B)	As SP1450B but screened to MIL-STD-883, Method 5004, Class B		177
SP1455B	140 Mbit/s PCM signal monitor		177
SP1455B(B)	As SP1455B but screened to MIL-STD-883, Method 5004, Class B		177
INTERFACE CIRCUITS			
SP1404BW **D3702**	High voltage interface	ITT7163	179
CMOS TELEPHONE DIALLING CIRCUITS — LOOP DISCONNECT			
MV4320	Keypad pulse dialler with M1 masking	DF320	85
MV4322	Keypad pulse dialler with M2 masking		85
MV4323	Keypad pulse dialler with selectable interdigit pause		85
MV4325	Programmable keypad pulse dialler with M1 masking		89
MV4326	Programmable keypad pulse dialler with M2 masking		89
MV4327	Programmable keypad pulse dialler with M1 and M2 masking		89

Quality data

Plessey Semiconductors has Factory Approval to:-

BS9300 for semiconductor devices of Assessed Quality (BSI Certificate 1053/M)

BS9400 for integrated circuits of Assessed Quality (BSI Certificate 1053/M)

CECC 50000 Inspection Organisation to document level 1 (BS9300) M0020/CECC refers

DEF STAN 05— 21.QC System requirements for Industry (Equivalent to AQAP— 1) Certificate 65752/1/01 refers

Devices are also manufactured and tested in accordance with the methods of **MIL-STD-833**, the US Military Standard; Test Methods and Procedures for Microcircuits, and **MIL-M-38510**, US Military Specification, Micro-electronics; General Specifications for.

DELIVERED PRODUCT QUALITY
It is our policy to deliver a relaible quality product and to achieve this end all devices undergo 100 % electrical testing of every relevant AC and DC parameter prior to shipment. The devices are tested under conditions of level and frequency closely simulating those of the typical application. Fully automatic Teradyne integrated circuit test machines, acknowledged to be among the best computer controlled test machines available, are employed.

Each and every stage of processing, assembly and testing is carefully audited by Plessey Semiconductors' independent Quality Assurance department.

Therefore we are able to guarantee the following Acceptable Quality Level (A.Q.L.) on all deliveries.

MECHANICAL
Defects of a mechanical nature including coding not being legible, deformed leads, dimensional tolerances being exceeded, wrong identification of pin 1 and pins not being solderable.

0.65 % AQL, I.L.II

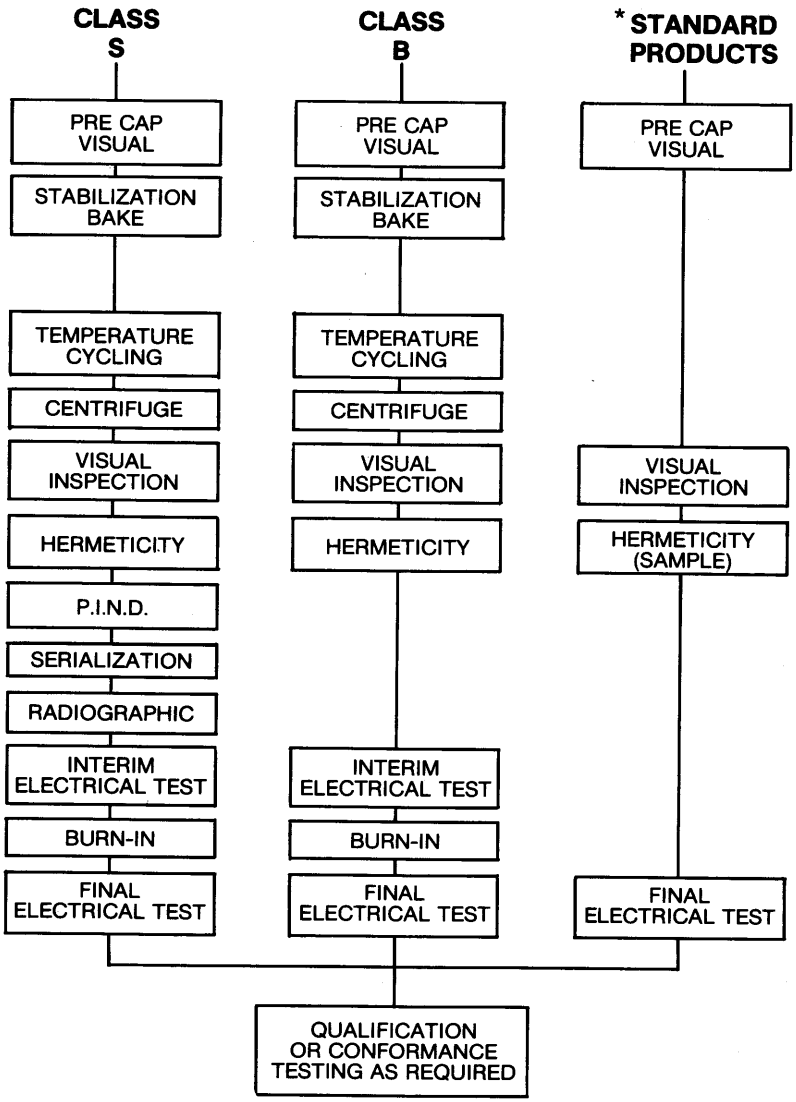
ELECTRICAL
Defects of an electrical nature including device parameters being outside the acceptance specification limits, or those only stated as typical being grossly in error.

0.4 % AQL, I.L.II

The average delivered product quality is considerably better than this, the population of imperfect devices being much smaller than that indicated by the AQL values.

Screening to MIL-STD-883

The following Screening Procedures are available from Plessey Semiconductors



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Technical Data

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MJ1410

8 BIT FORMAT CONVERTER

The MJ1410 is realised in N-channel MOS technology and operates from a single 5V supply. The circuit can be clocked from d.c. up to 2.5MHz and has 3-state output buffers capable of driving two LSTTL loads. All inputs are TTL compatible.

The MJ1410 performs the complementary functions of serial-to-parallel and parallel-to-serial data conversion on 8 bits of data. Both these conversions are achieved using the same time-position matrix, which has eight inputs and eight outputs.

An 8-bit parallel word clocked into the eight inputs appears as a serial 8-bit data stream on one of the eight outputs. Successive parallel words at the inputs appear as serial data streams on each of the eight outputs in turn.

Conversely, a serial 8-bit data stream on one of the eight inputs appears as an 8-bit parallel word on the eight outputs. Successive parallel words appearing at the eight outputs correspond to the serial data on each of the eight inputs in rotation.

The conversion can be 'programmed' to start in any register by setting the appropriate binary value on the counter pre-load inputs and applying a pulse to the Sync input. If the loading sequence produced by the counter is not required it can be disabled by connecting 'clock' to 'sync'. At each positive clock edge the register loaded will depend on the data on the counter inputs on the previous positive clock edge.

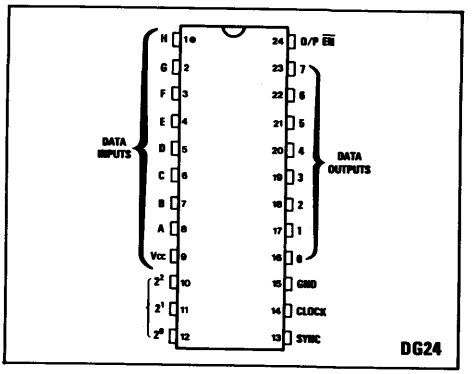

Fig.1 Pin connections

FEATURES

- Single 5V supply.
- Three-state outputs.
- All inputs TTL compatible.

FUNCTIONAL DESCRIPTION

Pin No.	Title	Function
1	H	Data i/p H
2	G	Data i/p G
3	F	Data i/p F
4	E	Data i/p E
5	D	Data i/p D
6	C	Data i/p C
7	B	Data i/p B
8	A	Data i/p A
	Data inputs	See Figs. 3 and 4
9	Vcc	Positive supply, 5V ± 5%
10	2^2	Counter preset i/p bit 2
11	2^1	Counter preset i/p bit 1
12	2^0	Counter preset i/p bit 0
		The counter is preset to the data on these i/ps on the 3rd positive clock edge following a negative edge on the 'sync' input.
13	SYNC	A negative edge on this i/p initiates the counter preset sequence which causes the conversion cycle to start in the register which corresponds to the binary value of the counter preset i/ps.
14	CLOCK	System clock
15	GND	Zero volts
16	0	Three state data o/p '0'
17	1	Three state data o/p '1'
18	2	Three state data o/p '2'
19	3	Three state data o/p '3'
20	4	Three state data o/p '4'
21	5	Three state data o/p '5'
22	6	Three state data o/p '6'
23	7	Three state data o/p '7'
	Data outputs	See Figs. 3 and 4
24	O/P $\overline{EN}$	A logic '1' on this i/p forces all the data outputs to a high impedance state.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated): V_{CC} = 5V, T_{amb} = 22°C ± 2°C, Test circuit: Fig. 6.
Supply voltage V_{CC} 5V ± 10%
Ambient operating temperature T_{amb} -10°C to +70°C

STATIC CHARACTERISTICS

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level I/P voltage	V_{IL}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	-0.3		0.8	Volts	
High level I/P voltage	V_{IH}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24	2.5		V_{CC}	Volts	
Low level I/P current/high level I/P current	I_{IN}	1,2,3,4, 5,6,7,8, 10,11,12, 13,14,24		1	50	µA	
Low level O/P voltage	V_{OL}	16,17,18, 19,20,21, 22,23			0.5	Volts	I_{SYNC} = 1.6mA
High level O/P voltage	V_{OH}	16,17,18, 19,20,21, 22,23	2.5			Volts	I_{SOURCE} = 100uA
Low level O/P current sync capability	I_{OL}	16,17,18, 19,20,21, 22,23	-1.6			mA	
High level O/P current source capability	I_{OH}	16,17,18, 19,20,21, 22,23	100			µA	
OFF state O/P current	$I_{OFF\ L}$	16,17,18, 19,20,21, 22,23			40	µA	V_{OUT} = GND
	$I_{OFF\ H}$	16,17,18, 19,20,21, 22,23			-40	µA	V_{OUT} = V_{CC}
Power dissipation	P_{DISS}		90		500	mW	V_{CC} = 5.5V

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max.clock frequency	$F_{max.}$	2.4		10	MHz	
Min. clock frequency	$F_{min.}$	0			MHz	
Sync. pulse width (positive)	t_{SPP}	60			ns	Fig. 6
Sync. pulse width (negative)	t_{SPN}	100			ns	Fig. 6
Lead of sync. clocking edge on positive clock edge	t_{SL}	130			ns	Fig. 6
Set up time of counter inputs (2^0,2^1,2^2)	t_{SC}	70			ns	Fig. 6
Hold time of counter inputs	t_{HC}	60			ns	Fig. 6
Set up time of data inputs (A-H)	t_{SD}	80			ns	Fig. 6

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Hold time of data inputs	t_{HD}	85			ns	Fig. 6
Propagation delay, data out valid from output $\overline{\text{ENABLE}}$ low	t_{PDE}			100	ns	Fig. 6
Propagation delay, data out disabled from output $\overline{\text{ENABLE}}$ high	t_{PDD}			100	ns	Fig. 6
Propagation delay, clock to data out valid	t_{PCD}			200	ns	Fig. 6

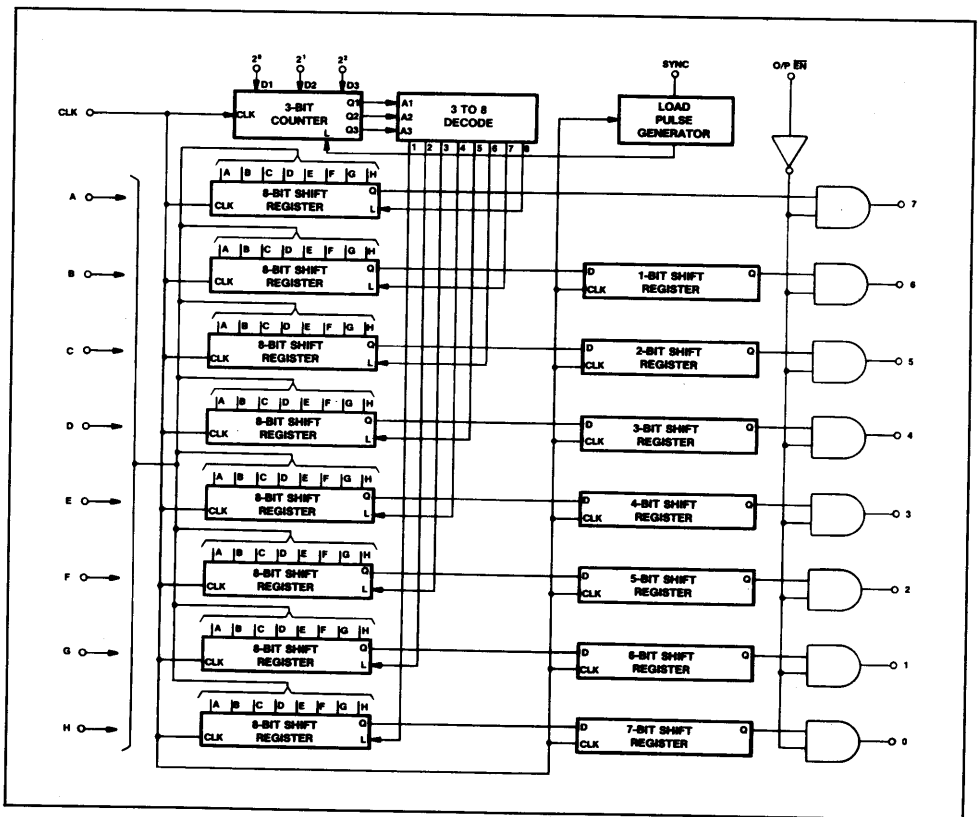

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin w.r.t. ground = 7V max.
Storage temperature = -55°C to +125°C

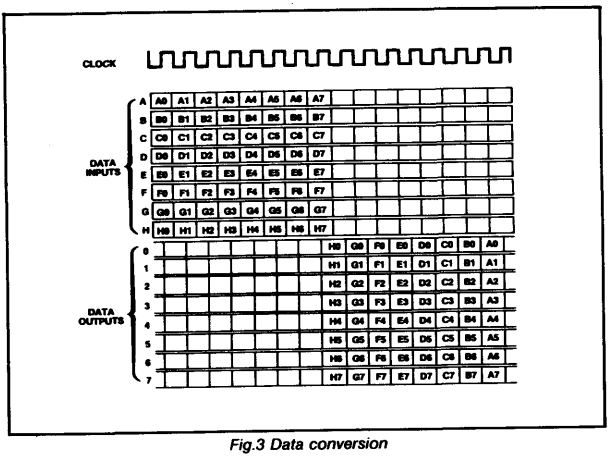

Fig.3 Data conversion

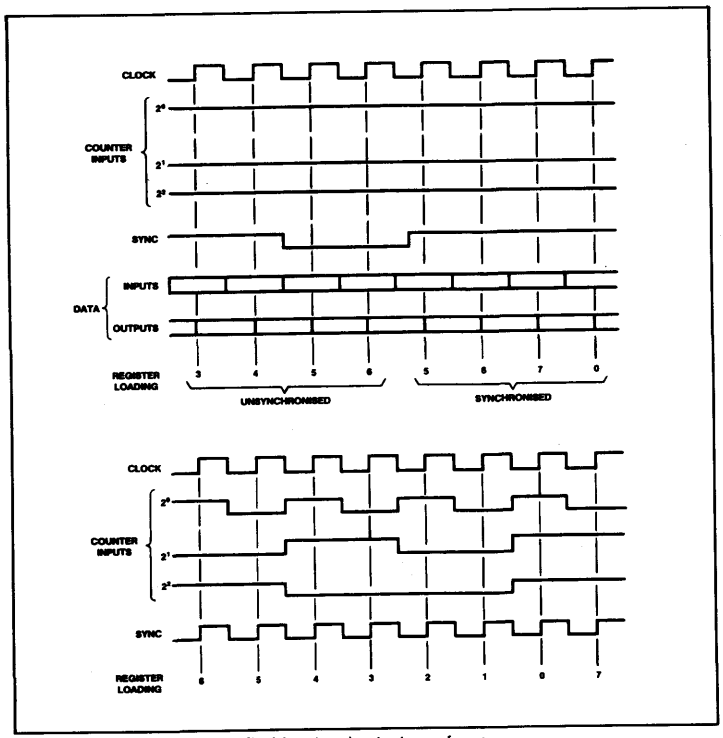

Fig.4 Input and output waveforms

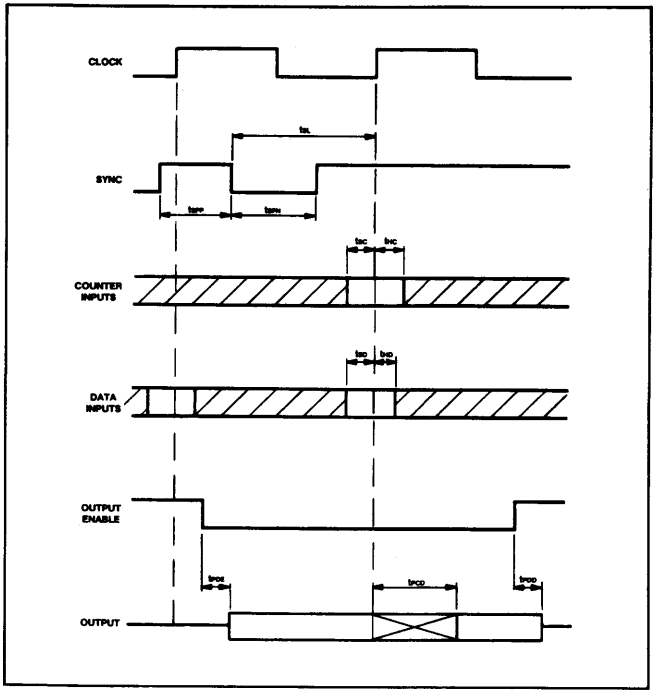

Fig.5 Timing details

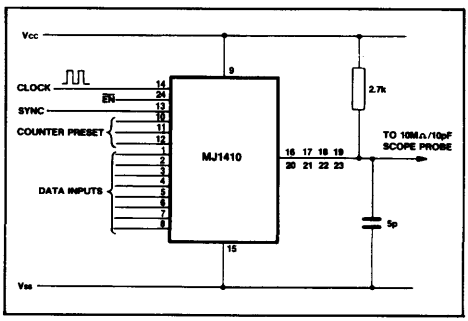

Fig.6 Test conditions

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2 MBIT PCM SIGNALLING CIRCUIT
MJ 1440
HDB3 ENCODER/DECODER

The 2.048 MBit PCM Signalling Circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply, relevant inputs and outputs are TTL compatible.

The MJ1440 is an encoder/decoder for the pseudo-ternary transmission code, HDB3 (CCITT Orange Book Vol III.2 Annex to Rec. G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding, all ones detection and loss of input (all zeroes detection). In addition a loop back function is provided for terminal testing.

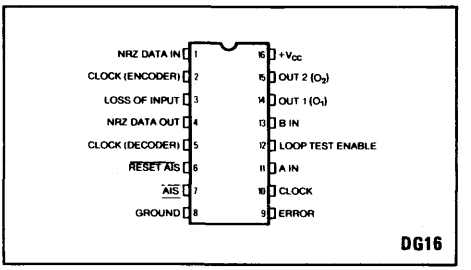

Fig. 1 Pin connections

FEATURES

- 5v ± 5% Supply – 50mA Max
- HDB3 Encoding and Decoding to CCITT rec. G703.
- Asynchronous Operation.
- Simultaneous Encoding and Decoding.
- Clock Recovery Signal Generated from Incoming HDB3 Data.
- Loop Back Control.
- HDB3 Error Monitor
- 'All Ones' Error Monitor
- Loss of Input Alarm (All Zeros Detector).
- Decode Data in NRZ Form.

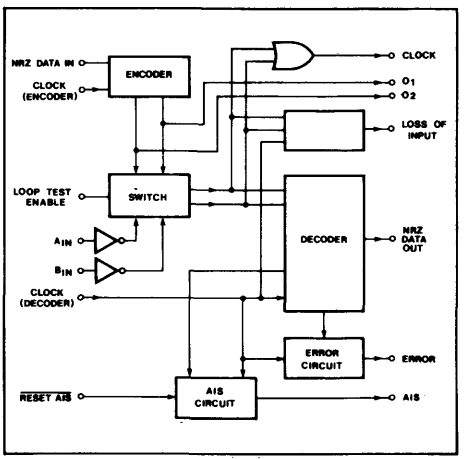

Fig. 2 Block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd – 0.3V
Outputs	Vcc, Gnd –0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance:	Chip to Case	Chip to Amb.
	40°C/Watt	120°C/Watt

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = 0°C$ to $+70°C$

Static characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,5,6 10,11,12,13	-0.3		0.8	V	
Low level input current	I_{IL}				50	µA	$V_{IL} = 0V$
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	µA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 80µA
		3,4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	3,4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	50	mA	All inputs to 0V All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0	10		MHz	Figs.10, 15
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2	5		MHz	Figs.11, 15
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.10, 15. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.10, 15
tpd1A-tpd1B				20	ns	Figs.10, 15
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = Figs.13, 15
Setup time of NRZ data in to Clock (Encoder)	ts3	30			ns	Figs.8, 10, 15
Hold time of NRZ data in	th3	55			ns	Figs.10, 15
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.9, 13, 15
Propagation delay Clock (Decoder) to loss of input				150	ns	
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.12, 15
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.14, 15
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.9, 11, 15. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.9, 11, 15
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.9, 11, 15
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs.9, 14, 15
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	200			ns	Figs.9, 14, 15
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.14, 15

NOTES
1. Encoded HDB3 outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4).

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1. NRZ Data in
Input data for encoding into ternary HDB3 form. The NRZ data is clocked by the negative edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1

3. Loss of input alarm
This output goes to logic '1' if eleven consecutive zeroes are detected in the incoming HDB3 data. The output is set to logic '0' on receipt of a '1'.

4. NRZ data out
Decoded data in NRZ form from ternary HDB3 input data (A_{in},B_{in}), data is clocked out by positive going edge of clock (Decoder).

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. Reset AIS, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on Reset AIS enables the internal decoded zero counter.

8. Ground
Zero volts

9. Error
A logic '1' indicates that a violation of the HDB3 coding has been received i.e. 3 '1's of the same polarity.

10. Clock
'OR' function of $\overline{A_{in}}$,$\overline{B_{in}}$ for clock regeneration when pin 12 = '0', 'OR' function of O_1,O_2 when pin 12 = '1'.

11,13. A_{in},B_{in}
Inputs representing the received ternary HDB3 PCM signal. A_{in} = '0' represents a positive going '1', B_{in} = '0' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the Clock (Decoder). A_{in} and B_{in} may be interchanged.

12. Loop test enable
Input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous. When pin 12 = '1' O_1 is connected internally to A_{in}. O_2 is connected internally to B_{in}. Clock becomes the OR function $O_1 + O_2$. The delay from NRZ in to NRZ out is 6½ clock periods in the loop back condition.

14, 15. O_1, O_2
Outputs representing the ternary encoded data for line transmission O_1 = '1' representing a positive going '1', O_2 = '1' represents a negative going '1'. O_1 and O_2 may be interchanged.

16. V_{cc}
Positive supply, 5V ± 5%

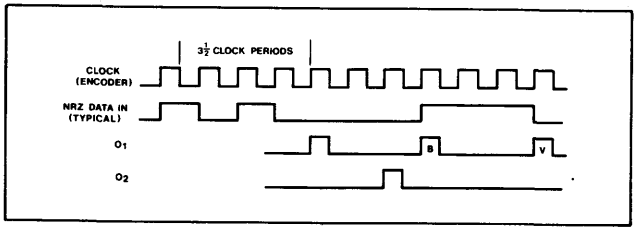

Fig. 3 Encode waveforms

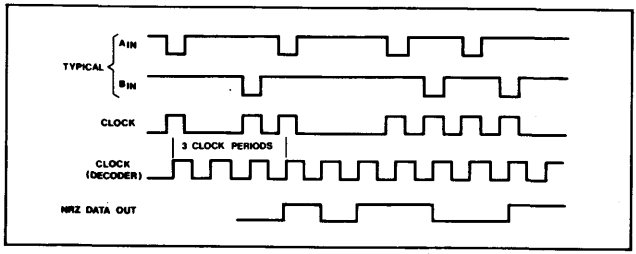

Fig. 4 Decode waveforms

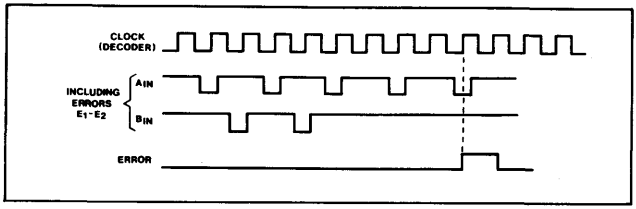

Fig. 5 HDB3 error output waveforms

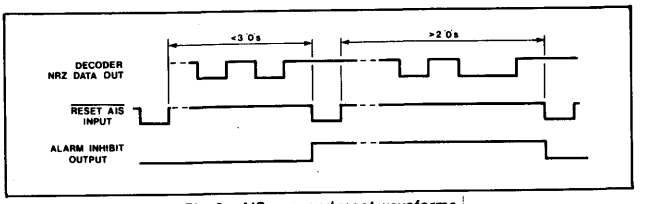

Fig. 6 AIS error and reset waveforms

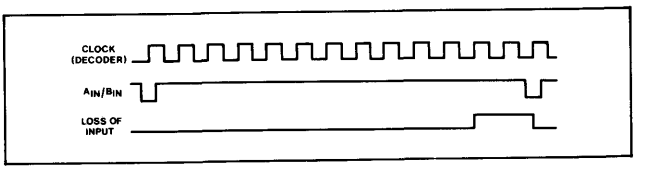

Fig. 7 Loss of input waveforms

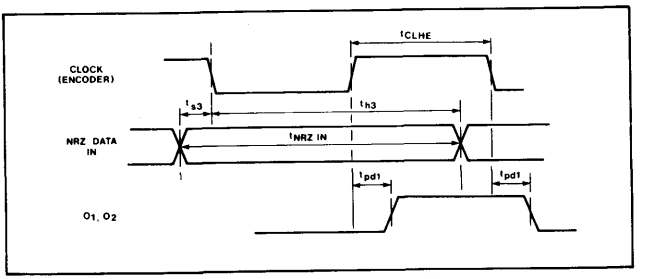

Fig. 8 Encoder timing relationship

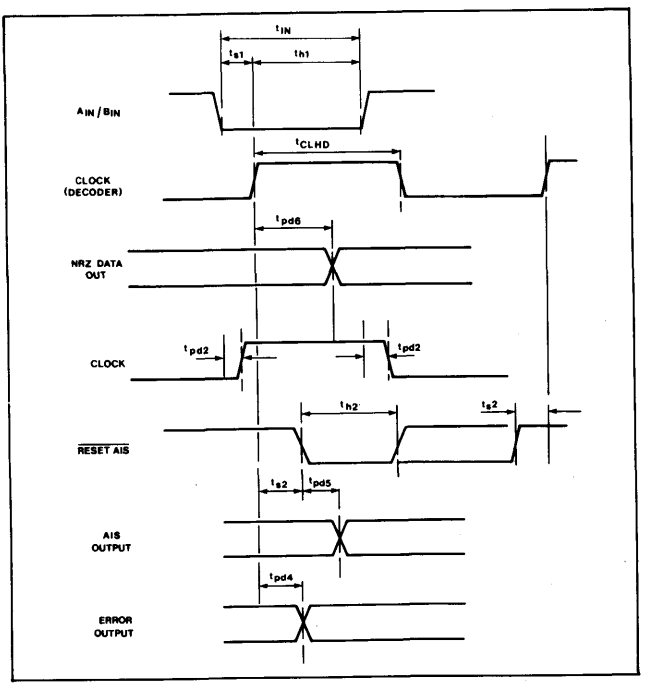

Fig. 9 Decoder timing relationship

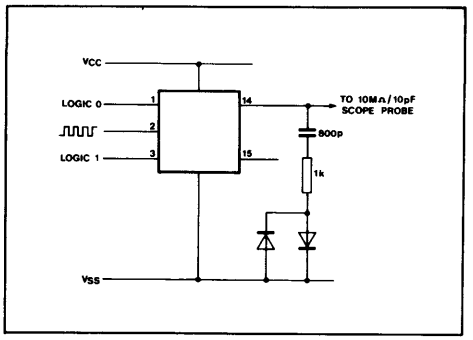

Fig. 10

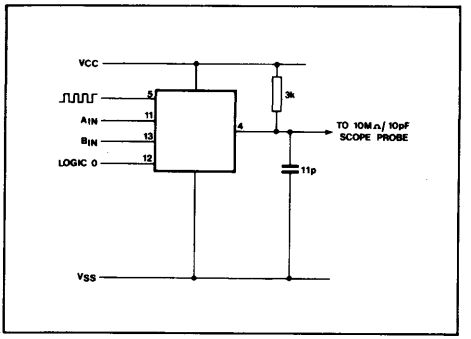

Fig. 11

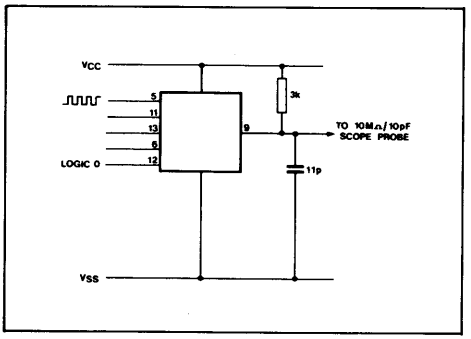

Fig. 12

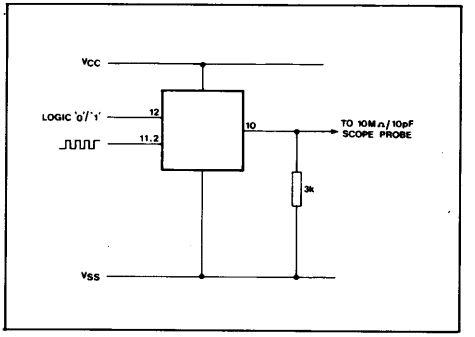

Fig. 13

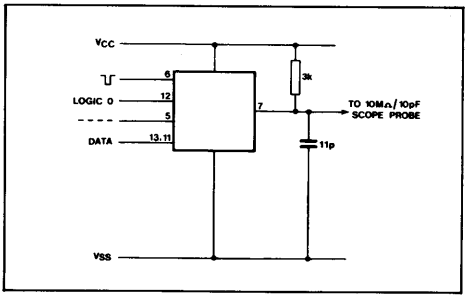

Fig. 14

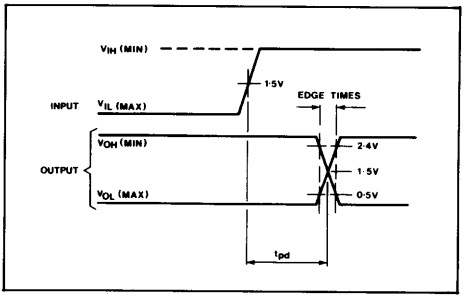

Fig. 15 *Test timing definitions*

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.
2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).
3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).
4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.
This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.
b The second and third spaces of a string are always coded as spaces.
c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

PLESSEY
Semiconductors

2 MBIT PCM SIGNALLING CIRCUIT

MJ 1444

PCM SYNCHRONISING WORD GENERATOR

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5 volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1444 generates the synchronising word in accordance with CCITT recommendations G732. The MJ1445 has been designed to detect this synchronising word when received at the remote end of the transmission system.

The synchronising word is injected onto the PCM data highway during time slot 0 in alternate frames. The spare time slot 0 data bits, bit 1 in every frame and bits 3 to 8 inclusive in alternate frames (i.e. those not containing the synchronising word) are available as parallel inputs and are output onto the PCM data highway.

The data output of the MJ1444 is 'open collector' and can be wire-OR'd directly onto the highway.

The device also provides a time slot 0 channel pulse 'TS0', time slot 0 non-sync. frame 'TS0 $\overline{SF}$', and time slot 16 'TS16' outputs.

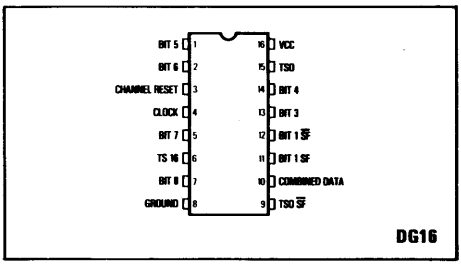

Fig.1 Pin connections

FEATURES

- 5V ± 5% Supply — 20 mA Typical
- Fully Conforms to CCITT Recommendation G732
- Outputs Directly Onto PCM Data Highway
- Provides Both Time Slot 0 and Time Slot 16 Channel Pulses
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

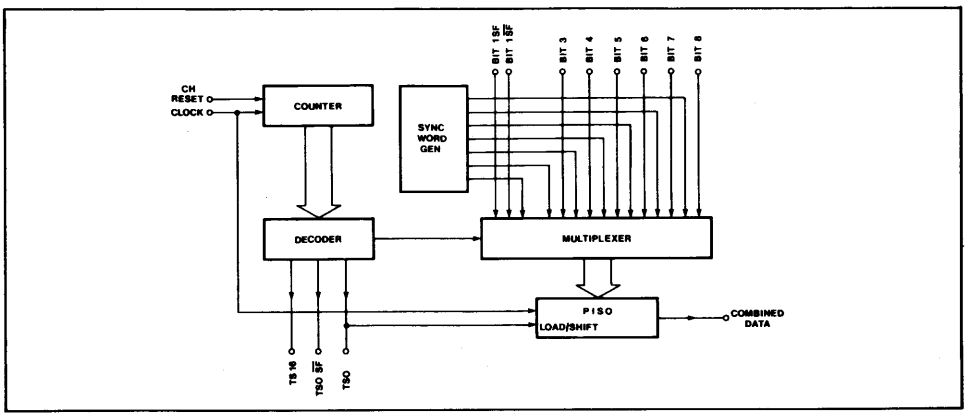

Fig.2 MJ1444 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient operating temperature $-10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	1, 2, 3, 4, 5, 7, 11, 12, 13, 14.	−0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}		
Low level output voltage	V_{OL}	6, 9, 15			0.5	V	$I_{sink} = 2mA$
		10			0.7	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	6, 9, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{OH}	10			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max clock frequency	F_{max}	3	5		MHz	
Propagation delay, clock to TS0, TS0 $\overline{SF}$, TS16 and combined data outputs.	t_p	80		200	ns	See Figs.5 and 6
Set up time channel reset to clock	T_{S1}	100		450	ns	$f_{clock} = 2.048MHz$
Hold time of channel reset input	t_{H1}	20		400	ns	
Set up time of bit 1 (SF) to datum B	t_{S2}	100			ns	
Hold time of bit 1 (SF) wrt datum B	t_{H2}	300			ns	
Set up time of bit 1 ($\overline{SF}$) and data bits 3—8 to datum B	t_{S2}	100			ns	
Hold time of bit 1 ($\overline{SF}$) and data bits 3—8 wrt datum B	t_{H2}	300			ns	

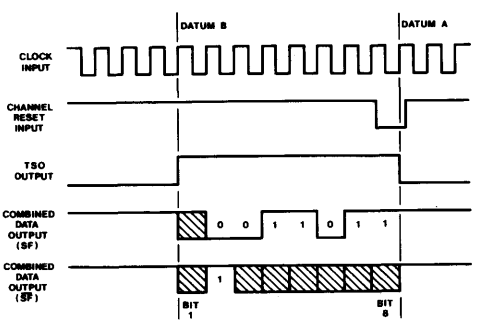

Fig.3 Data timing

FUNCTIONAL DESCRIPTION

Functions Listed by pin number

1, 2, 5, 7, 13, 14. Bits 3 to 8
Parallel data on these inputs is asynchronously loaded into bits 3 to 8 of the PISO shift register for transmission during Time slot 0 of non-sync. frames.

3. Channel Reset
A low going pulse at this input synchronises the MJ1444 with the other devices at the transmit end of the PCM link. It may be applied as a start pulse or repeated at the same instant in successive frames.

4. Clock
System clock input (2.048MHz for a 2 Mbit PCM system).

6. TS16
This output provides a positive pulse equivalent to 8 clock periods during time slot 16 of every 30 + 2 channel PCM frame.

8. GND
Zero volts.

9. TS0 $\overline{SF}$
This output provides a positive pulse equivalent to 8 clock periods during time slot 0 of non-sync. frames.

10. Combined data
This 'open collector' output injects the contents of the PISO shift register onto the PCM data highway during time slot 0 in successive frames. The contents of the PISO shift register are defined as follows:

	Bit 1	2	3	4	5	6	7	8
Sync. Frame	X	0	0	1	1	0	1	1
Non-sync. frame	X	1	X	X	X	X	X	X

X — indicates that these bits may be set according to the parallel data inputs.

11. Bit 1 SF
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of sync. frames.

12. Bit 1 $\overline{SF}$
Data on this input is asynchronously loaded into bit 1 of the PISO shift register for transmission during time slot 0 of non-sync. frames.

15. TS0
This output provides a positive pulse equivalent to 8 clock period during time slot 0 of every 30 channel PCM frame.

16. V_{CC}
Positive supply, 5V ±5%.

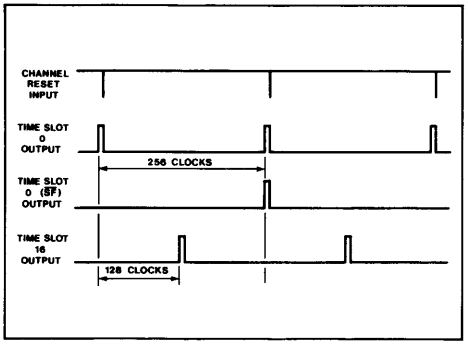

Fig.4 Sync. timing

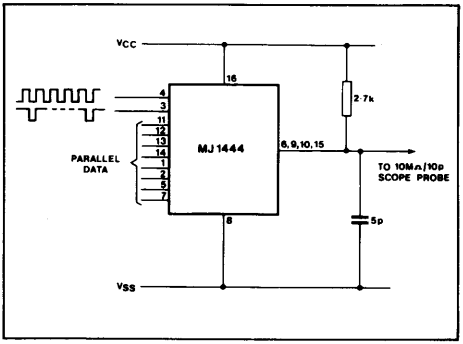

Fig.5 Test conditions (all outputs)

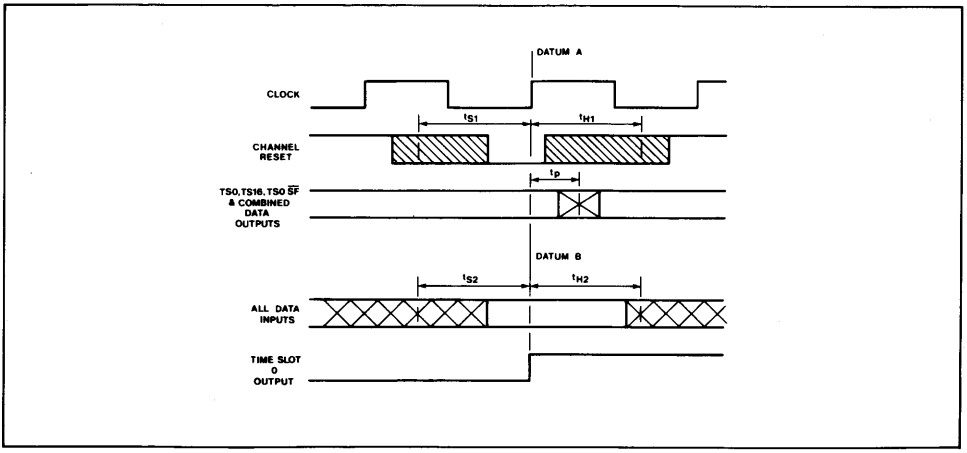

Fig.6 Timing definitions

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PCM SYNCHRONISING WORD RECEIVER

MJ1445

2 MBIT PCM SIGNALLING CIRCUIT

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 MBit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1445 establishes synchronisation by detecting the synchronising word when it is received at the remote end of the transmission system. The MJ1444 has been designed to generate this synchronisation word at the sending end of the system in accordance with CCITT recommendation G732.

Corruption of individual synchronisation words is signified by an 'Error' output, loss of synchronisation is indicated by a 'Sync Alarm' output and follows CCITT G732 in that loss of synchronism is assumed when 3 consecutive synchronisation words have been received with errors.

The 'Channel Reset' output goes low for the first period of the clock after time slot 0 in sync frames whenever the MJ1445 has established that the receiver terminal is in synchronisation in order that the rest of the receiver terminal may be reset.

The 'TSO' output is high for a period of 8 bits starting from the end of the first bit of the synchronising word. The spare data bits from the synchronising word are provided as parallel outputs.

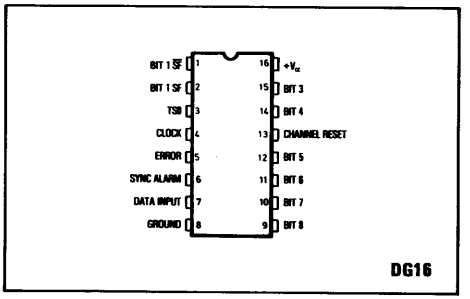

Fig.1 Pin connections

FEATURES

- 5V ±5% Supply - 20mA Typical.
- Conforms to CCITT Recommendation G732
- Synchronising Word Error Monitor
- Out of Sync. Alarm
- All Inputs and Outputs are TTL Compatible

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
35°C/Watt	120°C/Watt

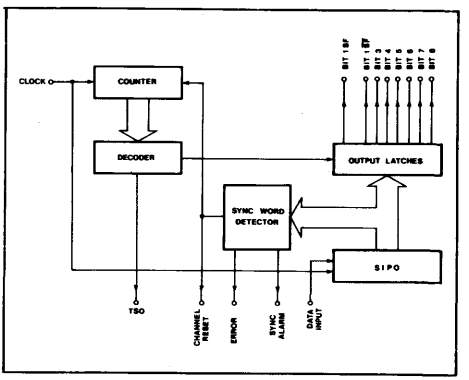

Fig.2 Block diagram MJ1445

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage, $V_{CC} = 5V \pm 0.25V$
Ambient temperature, $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	4, 7	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	4, 7		1	50	μA	
High level input voltage	V_{IH}	4, 7	2.4		V_{CC}	V	
Low level output voltage	V_{OL}	1, 2, 3, 5, 6 9, 10, 11, 12 13, 14, 15			0.5	V	$I_{sink} = 2mA$
High level output voltage	V_{OH}		2.8				$I_{source} = 200\mu A$
Supply current	I_{CC}			20	40	mA	$V_{CC} = 5.25V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. clock frequency	f_{max}	2.2	4.5		MHz	
Input delay of data input	$t_{d\ data}$	20		200	ns	$f_{clock} = 2.048MHz$
Propagation delay, clock to TS0 output	$t_{d\ TS0}$	40		200	ns	Fig.3
Propagation delay clock to error output, sync alarm and CH. Reset output high	t_d	50		400	ns	Fig.3
Propagation delay, clock to CH. Reset output low ($T - t_p$)	t_p	100		450	ns	Fig.3
Propagation delay clock to spare bits	$t_{d\ SB}$	50		300	ns	Fig.3

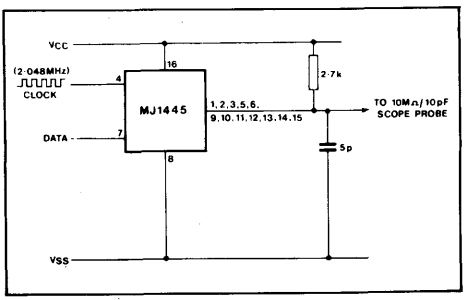

Fig.3 Test conditions, all outputs

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. Bit 1 $\overline{SF}$
This output is set to the level of data bit 1 during time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

2. Bit 1 SF
This output is set to the level of data bit 1 during time slot 0 of sync frames. The data becomes true on the first falling edge of the clock during TS1.

3. TS0
This output provides a positive pulse of 8 clock periods in every frame starting from the end of the first bit of the synchronising word of the received data.

4. Clock
System clock input (2.048MHz for a 2MBit PCM system).

5.Error
This output goes high at the end of time slot 0 in the 2nd sync frame following the frame with sync word errors. If consecutive sync words occur with errors this output will remain high. If a sync alarm is generated this output will remain high until sync is regained, but will always be low during bit 1 of TS1.

6. Sync Alarm
This output goes high at the end of time slot 0 output in the 3rd consecutive sync frame containing sync word errors. It returns low at the end of TS0 output in the 3rd consecutive frame received correctly (sync and non sync).

7. Data Input
Serial data (2MBit/s) at this input is clocked through the SIPO shift register and examined by the sync word detector.

8. GND
Zero volts

9, 10, 11, 12, 14, 15. Bits 3 to 8
These parallel outputs are set to the level of the spare data bits (3 to 8) of time slot 0 of non sync frames. The data becomes true on the first falling edge of the clock during TS1.

13. Channel reset
This output goes low for the first period of the clock after time slot 0 of the received data as long as synchronisation has been established. This pulse can be used to reset the rest of the receiver terminal.

16. V_{CC}
Positive supply $5V \pm 5\%$.

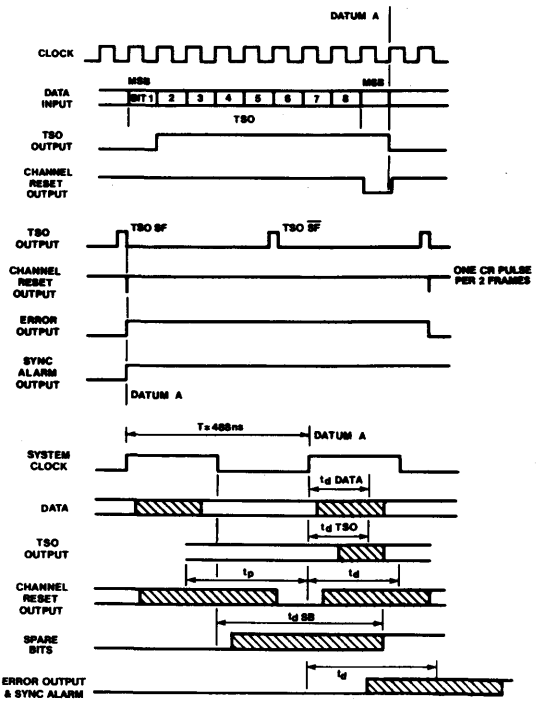

Fig.4 Timing diagram and output waveforms

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2 MBIT PCM SIGNALLING CIRCUIT

MJ1446

TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependent on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64kbits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

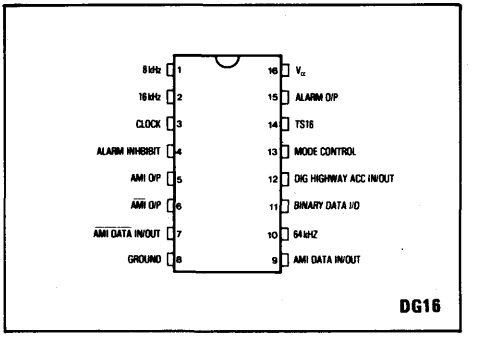

Fig.1 Pin connections

FEATURES

- 5V ±5% Supply — 20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receive or Transmit
- All Inputs and Outputs are TTL Compatible.

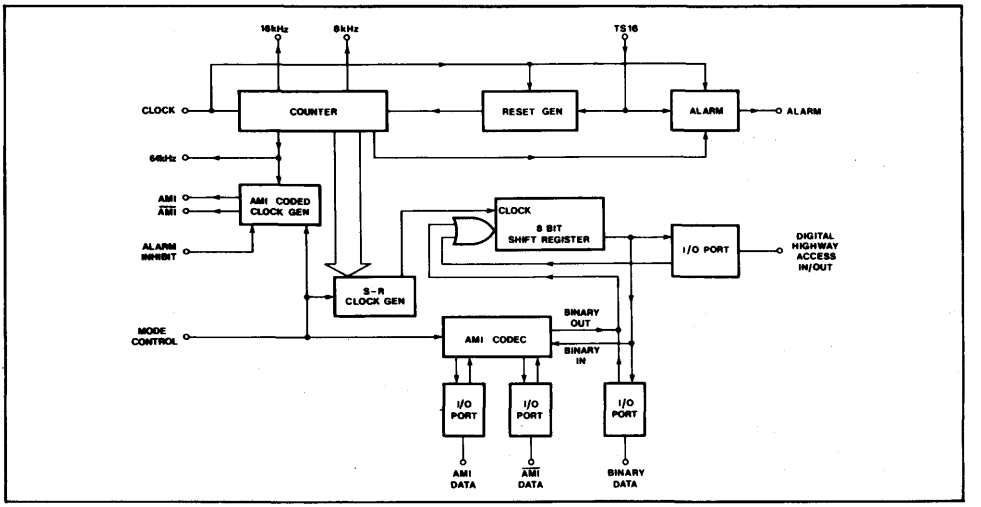

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = -10°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	μA	
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	$I_{sink} = 2mA$
		12			0.5	V	$I_{sink} = 5mA$
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	$I_{source} = 200\mu A$
High level output leakage current	I_{CH}	7, 9, 11, 12			20	μA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	$V_{CC} = 5.25V$

Dynamic Characteristics ($f_{clock} = 2.048$ MHz)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64 kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\,DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\,TS16}$	80		200	ns	
Output delay 64 kHz to 16 kHz output	$t_{p\,16}$			70	ns	Fig.7
Output delay, 64 kHz to 8 kHz output	$t_{p\,8}$			170	ns	Fig.7
Output delay, 64 kHz to binary data output (64 kHz)	$t_{p\,BIN}$	20		450	ns	Fig.8
Output delay 64 kHz to AMI, $\overline{\text{AMI}}$, AMI data & $\overline{\text{AMI}}$ data o/p's	$t_{p\,AMI}$	20		400	ns	Fig.8
Input delay, 64 kHz to binary data in (64 kHz)	$t_{d\,BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8 kHz
8kHz square wave output.

2. 16 kHz
16 kHz square wave output.

3. Clock
System clock input (2.048 MHz for a 2 Mbit PCM system)

4. Alarm inhibit
A high level on this input inhibits the 8 kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64 kHz.

6. $\overline{\text{AMI}}$ output

7. $\overline{\text{AMI}}$ Data in/out
In the transmit mode 64 kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

8. GND
Zero volts.

9. AMI Data in/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64 kbits/sec in AMI format.

10. 64 kHz
64 kHz square wave output.

11. Binary data in/out
In the transmit mode 64 k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64 k bits/sec in binary format.

12. Digital Highway access in/out
In the receive mode 2Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2Mbits/sec.

13. Mode control
A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16
This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output
A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}
Positive supply 5V ±5%.

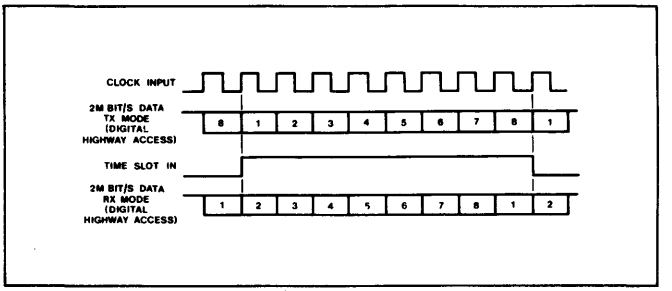

Fig.3 2MBit/s operation

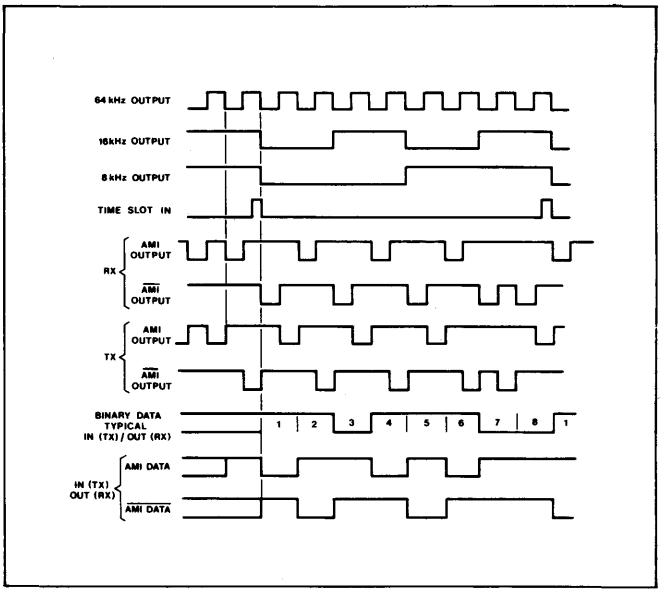

Fig.4 64kBit/s operation

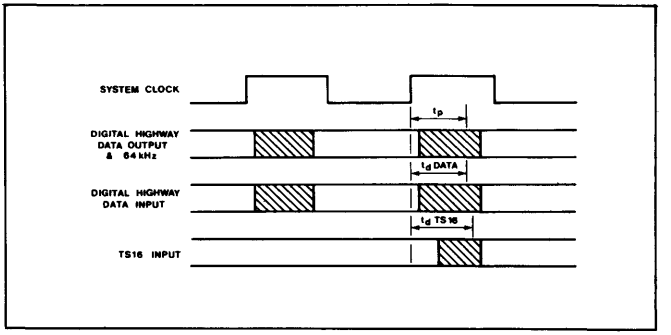

Fig.5 Timing diagram

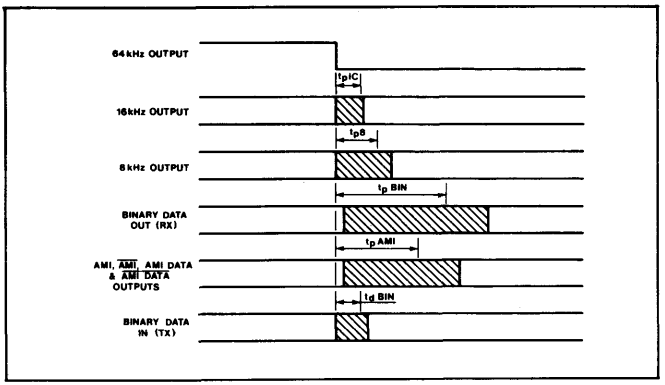

Fig.6 Timing diagram

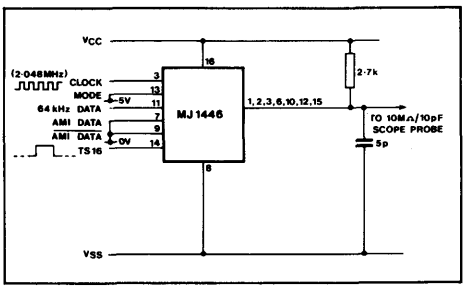

Fig.7 Test conditions (transmit mode)

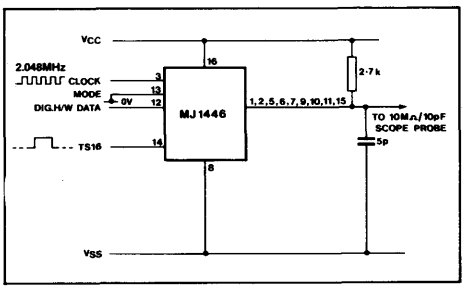

Fig.8 Test conditions (receive mode)

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2 MBIT PCM SIGNALLING CIRCUIT
MJ1471
HDB3 OR AMI ENCODER/DECODER

The MJ1471 is an encoder/decoder for pseudo-ternary transmission codes. The codes are true Alternate Mark Inversion (AMI) or AMI modified according to HDB3 rules (CCITT Orange Book Vol 111-2, Annex to Rec.G703). The device encodes and decodes simultaneously and asynchronously. Error monitoring functions are provided to detect violations of HDB3 coding and all ones detection (AIS). In addition a loop test function is provided for terminal testing.

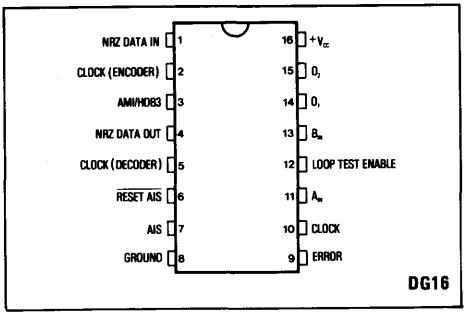

Fig.1 Pin connections

FUNCTIONS

- 5V ±5% Supply — 40mA Max.
- AMI or HDB3 Operation — TTL Selectable
- Loop Back Facility
- 'All Ones' Error Monitor to Detect Loss of Synchronising Word (Time Slot Zero)
- Error Monitor of HDB3 Incoming Code
- Decoded Data in NRZ Form

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. NRZ data in
Input data for encoding into ternary form. The data is clocked by the negative-going edge of the Clock (Encoder).

2. Clock (Encoder)
Clock for encoding data on pin 1.

3. AMI/HDB3
MJ1471 operates in HDB3 if pin 3 is at logic '1'. AMI if pin 3 is at logic '0'.

4. NRZ Data out
Decoded data from ternary inputs A_{in}, B_{in}.

5. Clock (Decoder)
Clock for decoding ternary data A_{in}, B_{in}.

6, 7. Reset AIS, AIS
Logic '0' on $\overline{\text{Reset AIS}}$ resets a decoded zero counter and either resets AIS outputs to zero provided 3 or more zeroes have been decoded in the preceding $\overline{\text{Reset AIS}}$ = 1 period or sets AIS to '1' if less than 3 zeroes have been decoded in the preceding two $\overline{\text{Reset AIS}}$ = 1 periods.
Logic '1' on $\overline{\text{Reset AIS}}$ enables the internal decoded zero counter.

8. Ground
Zero volts.

9. Error
A logic '1' indicates that a violation of the HDB3 encoding law has been decoded i.e. 3 '1's of the same polarity.

10. Clock
OR function of A_{in}, B_{in} for clock regeneration when pin 12 = '0', OR function of O_1 O_2 when pin 12 = '1'.

11, 13. A_{in}, B_{in}
Inputs representing the received ternary PCM signal. A_{in} = '1' represents a positive going '1', B_{in} = '1' represents a negative going '1'. A_{in} and B_{in} are sampled by the positive going edge of the clock decoder. A_{in} and B_{in} may be interchanged.

12. Loop test enable
TTL input to select normal or loop back operation. Pin 12 = '0' selects normal operation, encode and decode are independent and asynchronous.
When pin 12 = '1' O_1 is connected internally to A_{in} and O_2 to B_{in}. Clock becomes the OR function of O_1, O_2. **N.B.** a decode clock has to be supplied. The delay from NRZ in to NRZ out is 7½ clock periods in loop back.

14, 15, O_1, O_2
Outputs representing the ternary encoded PCM AMI/HDB3 signal for line transmission. O_1 and O_2 are in Return to zero form and are clocked out on the positive going edge of the encode clock. The length of O_1 and O_2 pulses is set by the positive clock pulse length.

16. $+V_{CC}$
Positive 5V ±5% supply.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage $V_{CC} = 5V \pm 0.25V$
Ambient temperature $T_{amb} = 0°C$ to $+70°C$

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min	Typ	Max		
Low level input voltage	V_{IL}	1,2,3,5,6 10,11,12,13	-0.3		0.8	volts	
Low level input current	I_{IL}				50	µA	$V_{IL} = 0V$
High level input voltage	V_{IH}		2.5		V_{cc}	V	
High level input current	I_{IH}				50	µA	$V_{IH} = 5V$
Low level output voltage	V_{OL}	10,14,15			0.5	V	Isink = 800µA
		4,7,9			0.4	V	Isink = 1.6mA
High level output voltage	V_{OH}	4,7,9	2.7			V	Isource = 60µA
		14,15	2.8			V	Isource = 2mA
		10	2.8			V	Isource = 1mA
Supply current	I_{cc}			20	40	mA	All inputs to 0v All outputs open circuit

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Clock (Encoder) frequency	$fmax_{enc}$	4.0	10		MHz	Figs.9, 14
Max. Clock (Decoder) frequency	$fmax_{dec}$	2.2	5		MHz	Figs.10, 14
Propagation delay Clock (Encoder) to O_1, O_2	tpd1A/B			100	ns	Figs.8, 9, 14. See Note 1
Rise and Fall times O_1, O_2				20	ns	Figs.9, 14
tpd1A-tpd1B				20	ns	Figs.9, 14
Propagation delay Clock (Encoder) to Clock	tpd3			150	ns	Loop test enable = 1, Figs.9, 14
Setup time of NRZ data in to Clock (Encoder)	ts3	30			ns	Figs.7, 9, 14
Hold time of NRZ data in	th3	55			ns	Figs.7, 9, 14
Propagation delay A_{in}, B_{in} to Clock	tpd2			150	ns	Loop test enable = '0' Figs.12, 14
Propagation delay Clock (Decoder) to error	tpd4			200	ns	Figs.11, 14
Propagation delay $\overline{\text{Reset AIS}}$ to AIS	tpd5			200	ns	Loop test enable = '0' Figs.13, 14
Propagation delay Clock (Decoder) to NRZ data out	tpd6			150	ns	Figs.7, 10, 14. See Note 2
Setup time of A_{in}, B_{in} to Clock (Decoder)	ts1	75			ns	Figs.7, 10, 14
Hold time of A_{in}, B_{in} to Clock (Decoder)	th1	5			ns	Figs.7, 10, 14
Hold time of $\overline{\text{Reset AIS}}$ = '0'	th2	100			ns	Figs.7, 13, 14
Setup time Clock (Decoder) to $\overline{\text{Reset AIS}}$	ts2	200			ns	Figs.7, 13, 14
Setup time $\overline{\text{Reset AIS}}$ = 1 to Clock (Decoder)	ts2'	0			ns	Figs.13, 14

NOTES
1. The Encoded ternary outputs (O_1, O_2) are delayed by 3½ clock periods from NRZ data in (Fig.3).
2. The decoded NRZ output is delayed by 3 clock periods from the HDB3 inputs (A_{IN}, B_{IN}) (Fig.4).

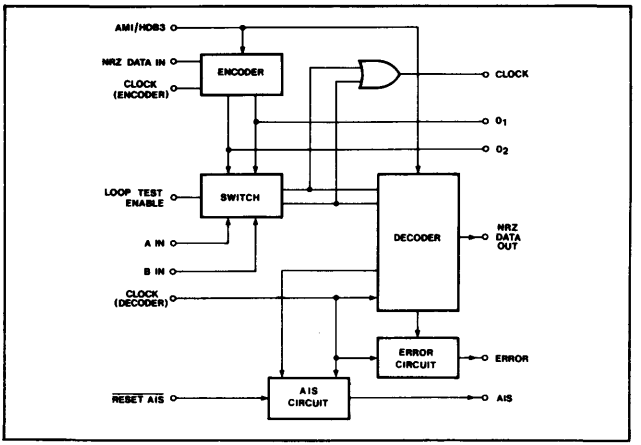

Fig. 2 MJ1471 Block diagram

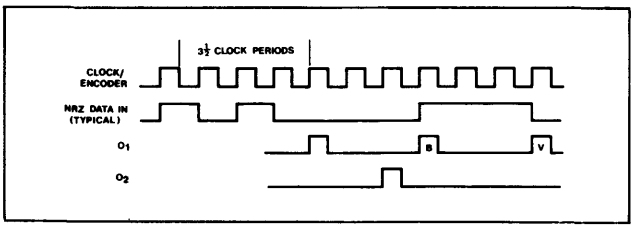

Fig. 3 Encode waveforms

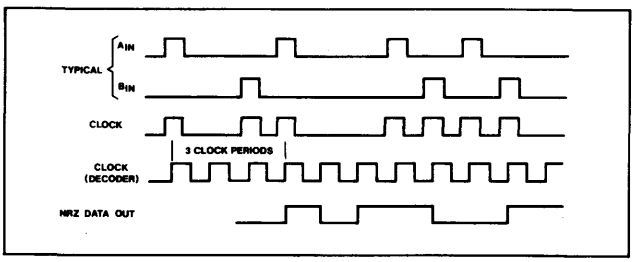

Fig. 4 Decode waveforms

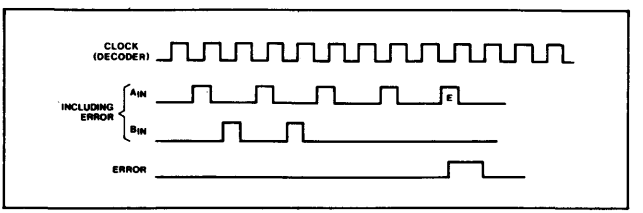

Fig. 5 HDB3 error output waveforms

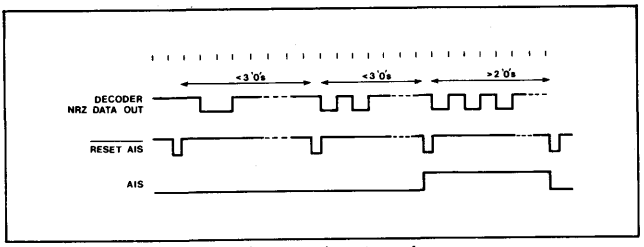

Fig.6 A/S error and reset waveforms

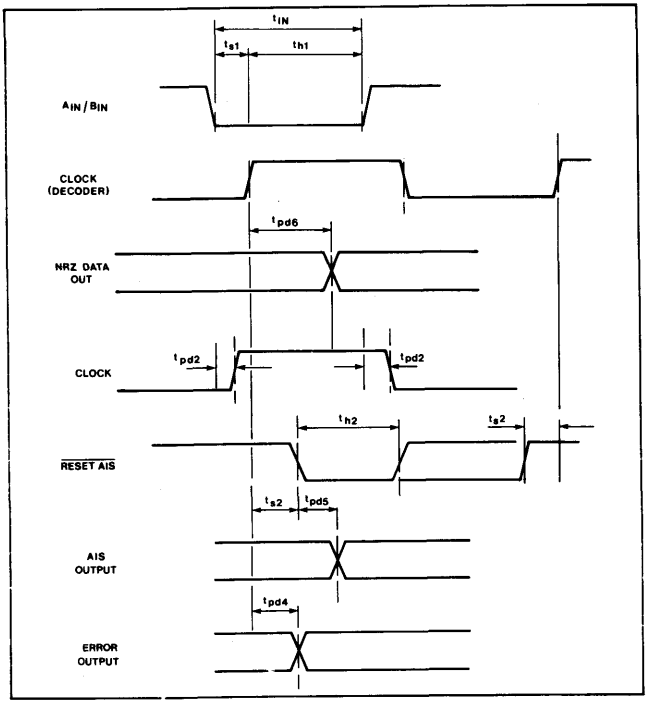

Fig. 7 Decoder timing relationship

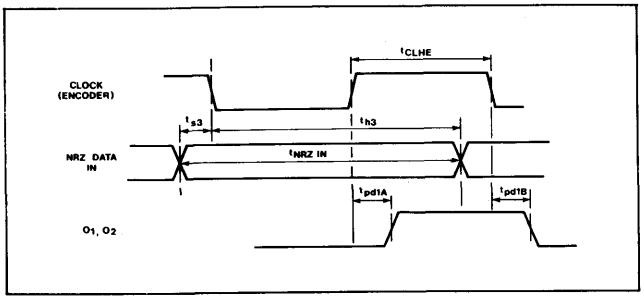

Fig. 8 Encoder timing relationship

DEFINITION OF THE HDB3 CODE

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. The HDB3 signal is psuedo-ternary; the three states are denoted B_+, B_- and O.
2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces however, special rules apply (see 4. below).
3. Marks in the binary signal are coded alternately as B_+ and B_- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (see 4. below).
4. Strings of four spaces in the binary signal are coded according to the following rules:

a The first space of a string is coded as a space if the preceding mark of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as a mark, i.e. not a violation (i.e. B_+, B_-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.
This rule ensures that successive violations are of alternative polarity so that no DC component is introduced.

b The second and third spaces of a string are always coded as spaces.

c The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V_+ or V_- according to their polarity.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Electrical Ratings

+Vcc	7V
Inputs	Vcc + 0.5V Gnd − 0.3V
Outputs	Vcc, Gnd −0.3V

Thermal Ratings

Max Junction Temperature 175°C

Thermal Resistance: Chip to Case	Chip to Amb.
40°C/Watt	120°C/Watt

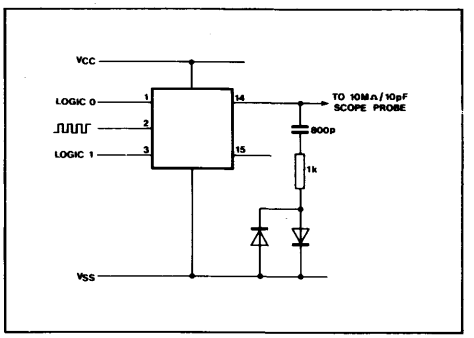

Fig. 9

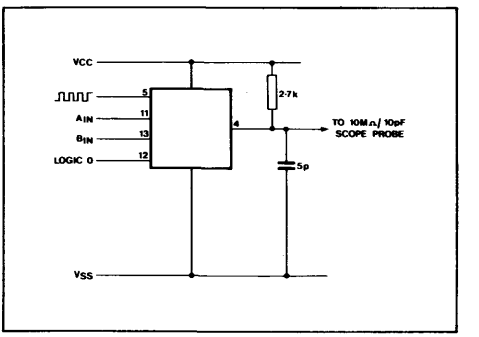

Fig. 10

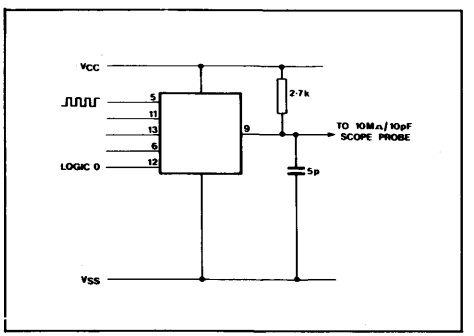

Fig. 11

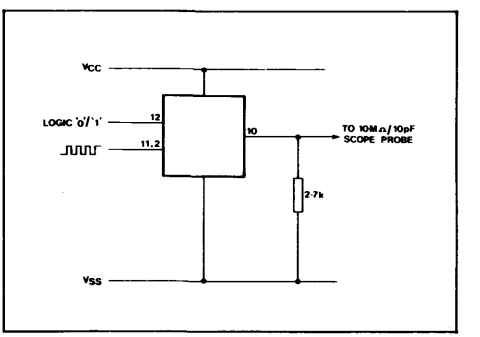

Fig. 12

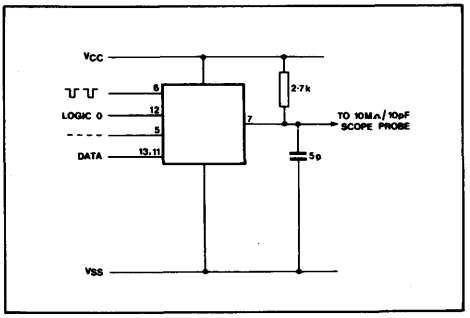

Fig. 13

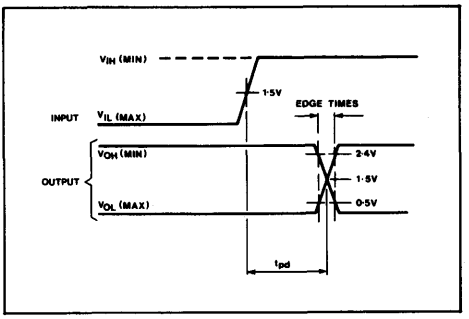

Fig. 14 Test timing definitions

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ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MJ1472

PCM RECEIVING CIRCUIT

The MJ1471/1742/1473 circuits have been designed specifically for use in 30 channel PCM systems. All circuits conform to the appropriate CCITT recommendations. The range of circuits is realised in N-channel MOS technology. They all operate from a single 5V supply and all inputs and outputs are TTL compatible. Operating speed of 2.048MHz is guaranteed over 0°C to 70°C temperature range.

The MJ1472 block diagram is shown in Figure 2.

FEATURES

- Line Time Generation (From 9 Stage Clock Driven Counter)
- Line Timing, Frame Alignment
- Alarm Signals FAT + MIR, ATL, AW, EPAT
- Test Points TP1, TP2, TP3, MR
- Inputs and Outputs LSTTL Compatible

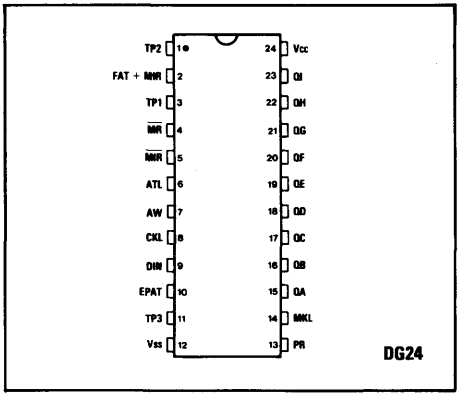

Fig.1 Pin connections (top view)

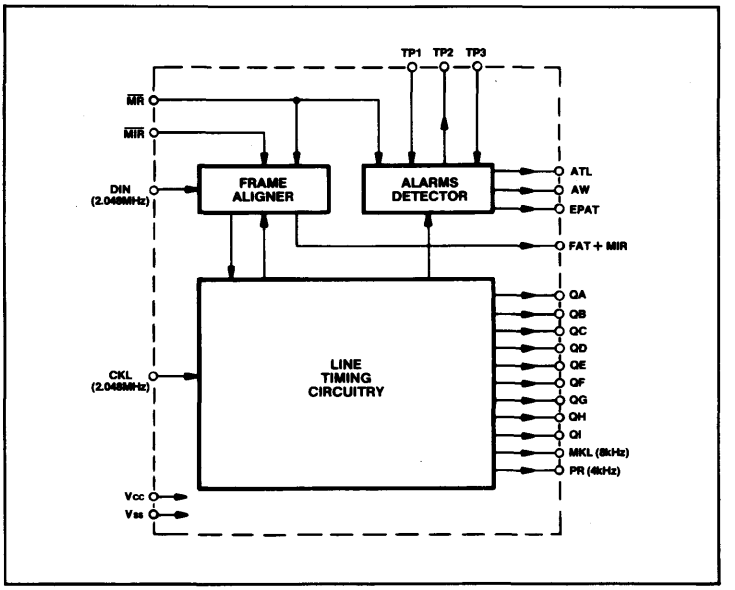

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0° C to +70° C
Package thermal resistance 60° C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	All inputs	2.7			V	I_{OH} -60μA
Low-level output voltage	V_{OL}	All inputs			0.5	V	I_{OL} = 0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25° C
High-level output current	I_{OH}	All outputs	-60			μA	V_{OH} = 2.7V
Low-level output current	I_{OL}	All outputs	0.8			mA	V_{OL} = 0.5V
Input capacitance	C_{IN}	All inputs			10	pF	1MHz 100mV
Supply current	I_{CC}			40	60	mA	V_{CC} = 5.25V

AC CHARACTERISTICS

Propagation delays	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Q_A to Q_I	t_{pd1}			50	ns	Fig 5 for loading Measure from CKL LE
MKL & PR	t_{pd2}			100	ns	As above
ATL & FAT + MIR	t_{pd3}			100	ns	As above
AW	t_{pd4}			300	ns	As above
EPAT	t_{pd5}			100	ns	Fig 5 for loading Measure from TP3 LE
TP2	t_{pd6}			150	ns	Fig 5 for loading Measure from TP1 TE
TP2	t_{pd7}			250	ns	Fig 5 for loading Measure from CKL LE
Required delay from DIN transition to CKE TE	t_1	50		430	ns	

FRAME ALIGNMENT

Frame alignment is described by the flow chart of Figure 3 where the A and B words are defined.

Position	1	2	3	4	5	6	7	8
Word A	X	0	0	1	1	0	1	1
Word B	X	1	X	X	X	X	X	X

Table 1

A(TA) represents the presence of word A in TSO of frame TA. B(TB) likewise represents the presence of word B in TSO of frame TB. $\bar{A}$(TA) and $\bar{B}$(TB) represent the absence of the words in TSO of the respective frame.

Frame alignment is assumed lost when 3 consecutive words A(TA) or B(TB) have been received with error. Frame alignment is recovered when the following sequence is detected in successive frames. Word A → word B (TB) and finally A(TA). To avoid the possibility of a state in which no frame alignment can be achieved due to the presence of an imitative frame alignment signal, the following procedure is followed. Should A(TA) be followed by absence of word B(TB) a new search for A is started a frame later.

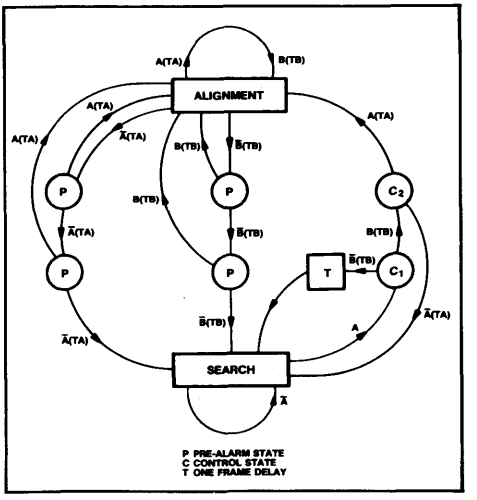

Fig.3 Frame alignment procedure

LINE TIMING

Nine stage clock (CKL) driven counter. All outputs (QA to QI) available externally.

MKL One bit positive pulse corresponding to 8th bit of TS15.

PR One bit positive pulse corresponding to position 8 of TS30 of frame A.

TRANSMISSION ALARM DETECTION

As already outlined in Fig.3. Three consecutive words A(TA) or B(TB) set an R-S flip-flop. This condition can also be forced by the external signal MIR.

MIR Input to R-S flip-flop.

FAT + MIR Output indication of state of R-S flip-flop.

ATL Output high when logic '1' is detected in position 3 of TS0, TB for two consecutive TB frames. Output low when logic '0' is detected in position 3 of TS0, TB. ATL output inhibited by the presence of output FAT + MIR.

AW Output high whenever $\bar{A}$(TA) is detected. Output is removed only when word $\bar{A}$(TA) is detected.

EPAT The output is high when for eight consecutive times at least 15 words A(TA) are detected in 512ms. EPAT alarm is removed (EPAT = 0) when less than 15 $\bar{A}$(TA) words are detected in (512 x 8)ms. The 512ms timer interval is obtained by an 11 bit binary counter clocked every double frame.

TEST POINTS

TP1, TP2, TP3 and Master Reset MR are test points.

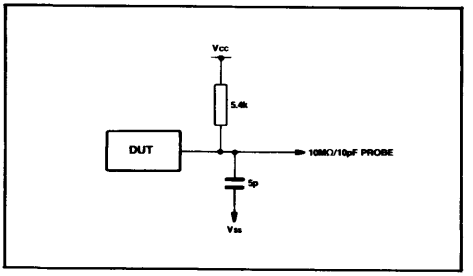

Fig.4 Propagation delay test circuit

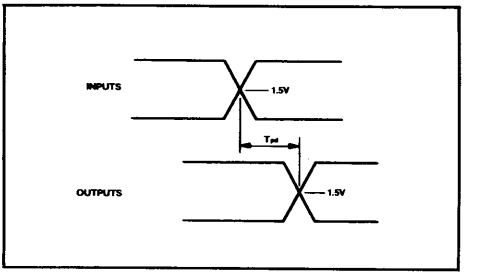

Fig.5 Waveforms for tpd

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MJ1473

PCM TRANSMITTER CIRCUIT

The MJ1400 Series of circuits have been specifically designed for use in 30 channel PCM systems.

The MJ1473 is designed to simplify the transmit section of a 30 channel, 2 MBit PCM link by converting NRZ PCM data to either AMI or HDB3 format after inserting a synchronising word in channel 0 (conforming to CCITT recommendations G.703 and G.732).

The data is output in pseudo-ternary form to facilitate driving the line interface via a transformer and AMI or HDB3 code may be remotely selected using bits 2 and 3 in channel 0 of the incoming data stream.

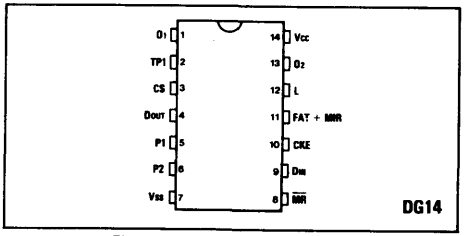


Fig.1 Pin connections - top view

FEATURES

- 5V - 30mA Power Requirements
- 0-70°C Operation
- Complies with Relevant CCITT Recommendations
- Control Signals Compatible with MJ1472,4
- NRZ, AMI or HDB3 Transmission Format
- Transmission Format Controlled Locally or Remotely Via TSO Data
- Fabricated in NMOS Technology
- Inputs and Outputs TTL Compatible

Bit	1	2	3	4	5	6	7	8
Channel 0 TS0.TA	X	0	0	1	1	0	1	1
Channel 0 TS0.TB	X	1	ATL	X	X	X	X	X

Table 1

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss : 7V
Storage temperature : -55° C to +155° C

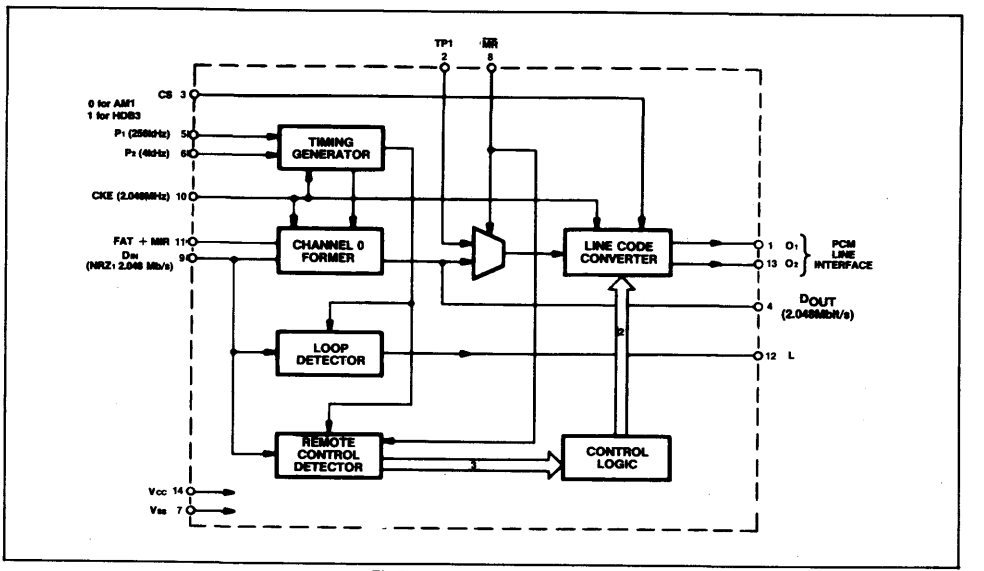


Fig.2 Block diagram of MJ1474

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0°C to +70°C
Package thermal resistance 95°C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	Outputs L & D_{OUT}	2.7			V	-60μA
Low-level output voltage	V_{OL}	Outputs L & D_{OUT}			0.5	V	0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25°C
High-level output current	I_{OH1}	Outputs L & D_{OUT}	60			μA	V_{OH} = 2.7V
High-level output current	I_{OH2}	Outputs O_1 & O_2	2			mA	V_{OH} = 2.8V
Low-level output current	I_{OL}	Outputs L & D_{OUT}	0.8			mA	V_{OH} = 0.5V
Input capacitance	C_{IN1}	All inputs except CKE			10	pF	1MHz 100mV
	C_{IN2}	Input CKE			20	pF	
Supply current	I_{CC}			30	45	mA	V_{CC} = 5.25V

AC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
O_1 & O_2	t_{pd1}			100	ns	Fig. 4 for loading; measure from CKE leading edge. See Fig. 5 for definition: total delay in t_{pd1} + 4 CKE periods.
L (Propagation delays)	t_{pd2}			200	ns	Fig. 3 for loading; measure from CKE trailing edge. See Fig. 5 for definition.
D_{OUT}	t_{pd3}			180	ns	Fig. 3 for loading; measure from CKE leading edge. See Fig. 5 for definition: total delay is t_{pd3} + 8 CKE periods.
Rise and fall times of O_1 & O_2	t_r/t_f			20	ns	Fig. 4 for loading. Measured between 0.5V and 2.4V points.
Required delay from D_{IN} P1.P2 transition to CKE TE	t_1	50		430	ns	
Required delay from FAT + MIR transition to CKE LE	t_2	50		430	ns	
Required delay from CS transition to CKE TE	t_3	50		430	ns	

CIRCUIT DESCRIPTION

The MJ1473 generates exchange timing by a synchronous 9-bit counter driven by exchange clock CKE and preset by P1,P2. The exchange clock also clocks data, D_{IN}, through the channel 0 former and to D_{OUT} via an eight bit shift register. In the channel 0 former, data bits of channel 0 are modified as shown in Table 1.

An X in Table 1 indicates transparency through the circuit, bits 2 and 3 of the shift register are concerned with the loop command circuitry. When '01' is detected an internal latch is set and the loop condition on output L is registered.

D_{OUT} may also be routed through the HDB3/AMI Encoder. The CS control is logic '0' for AMI and logic '1' for HDB3. Encoded data is then output to O_1 and O_2 in a form suitable for driving the PCM interface.

The line code converter can also be controlled by the remote control commands present on bits 2 and 3 of the shift register. These commands are as follows:

1. The presence of '00' in the first frame yields AMI transmission except channel 0 and 1, which are transmitted in a code determined by CS.
   The presence of '00' in each consecutive frame yields unipolar transmission except in channel 0 and 1 as above. The polarity of unipolar transmission is constant for any number of consecutive '00' frames but will alternate with respect to the previous unipolar transmission provided there has been an intermediate frame where '00' was not detected.
2. The presence of '11' in any frame yields AMI transmission except for channel 0 and 1 which are transmitted in a code determined by CS.

ATL is forced to a '1' by the presence of the external signal FAT + MIR, or by the presence of one of the two remote control commands or by the loop comand.

An 'all ones' condition on the encoded data outputs (O_1 O_2) is forced in the presence of a '1' in position 4 of channel 0, when the loop condition is met.

For normal operation $\overline{MR}$ = TP1 = 1. The test point TP1 is provided as an input independent of the line code converter. In order to enable this input MR = 0.

All inputs and outputs are compatible with LSTTL.

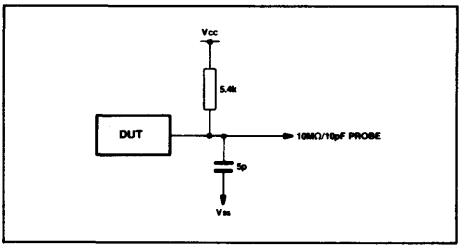


Fig.3 Propagation delay test circuits

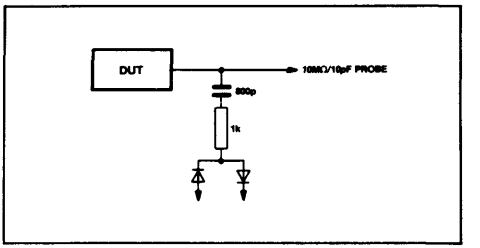


Fig.4

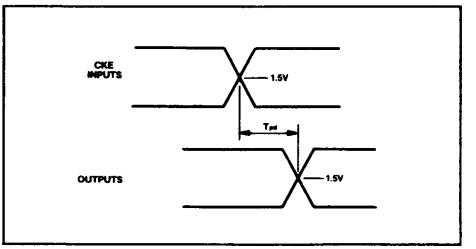


Fig.5 Waveforms for t_{pd}

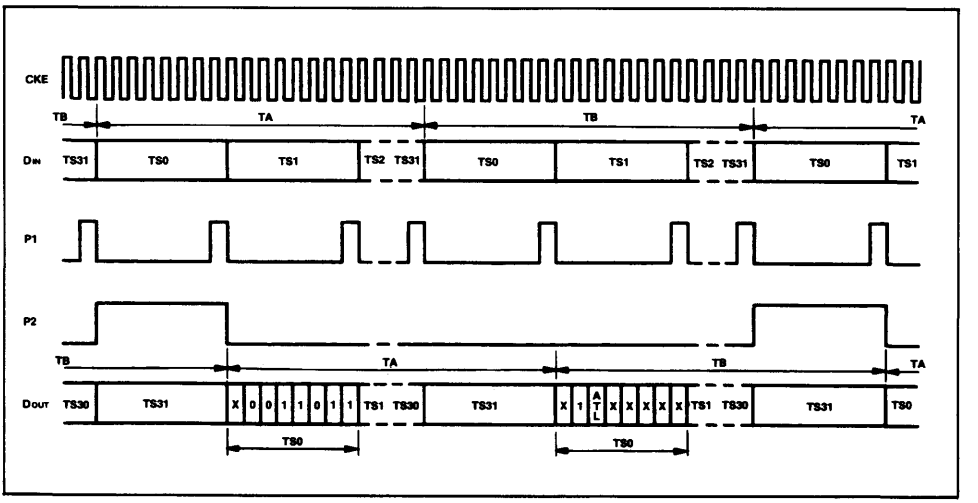


Fig.6 Timing diagram

PLESSEY
Semiconductors

ADVANCE INFORMATION

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have '*pre-production*' status. Details given may, therefore, change without notice although we would expect this performance data to be representative of '*full production*' status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MJ1474

PCM ELASTIC STORE

The MJ1400 Series of circuits have been specifically designed for use in 30 channel PCM systems.

The MJ1474 retimes the received 30 (+2) channel PCM data stream to the exchange clock and also produces a 5-bit output which identifies the individual channels within the retimed data stream.

Slip is handled by control logic which causes a repetition (or jump) of channel 0 for two consecutive frames whenever the Store capacity is about to be exceeded.

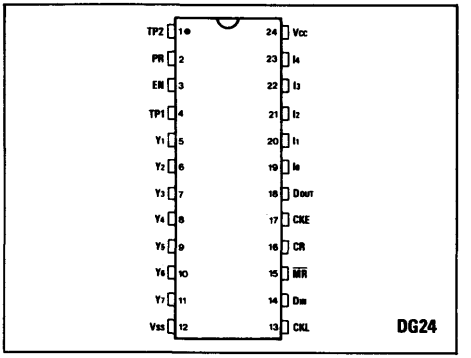


Fig.1 Pin connections - top view

FEATURES

- 5V - 50mA Power Requirements
- Performance Guaranteed Over 0-70°C Temperature Range
- Performs Slip/Alignment Function in 2.048 MBit PCM Systems
- Conforms to Relevant CCITT Recommendations
- Compatible with MJ1472, 3 Control Formats
- Fabricated in NMOS Technology
- Inputs and Outputs TTL Compatible

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to Vss : 7V
Storage temperature : -55°C to +155°C

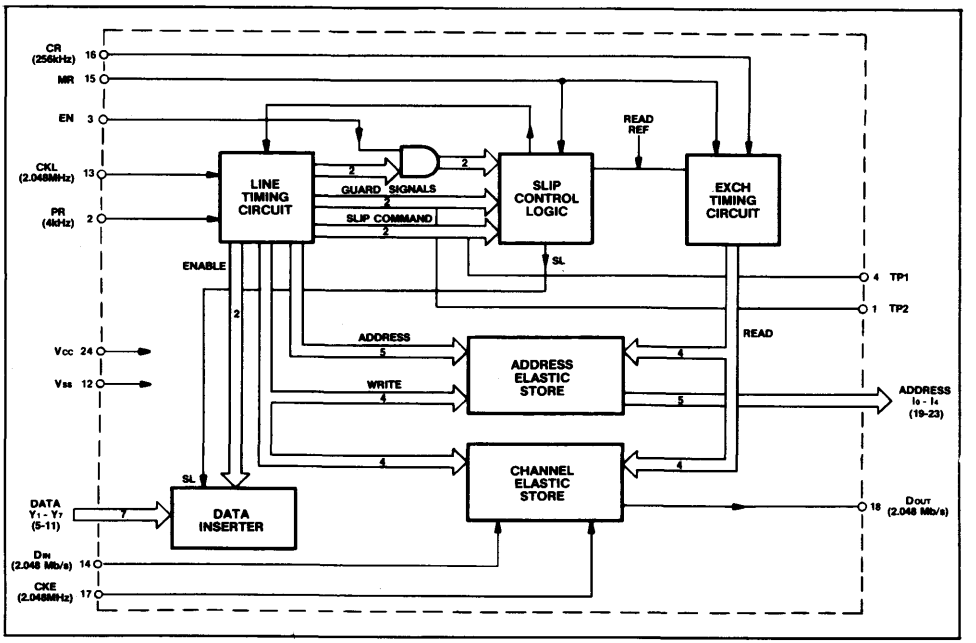


Fig. 2 Block diagram of MJ1473

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 5V ± 0.25V
Ambient operating temperature 0° C to +70° C
Package thermal resistance 60° C/watt

DC CHARACTERISTICS

Characteristic	Symbol	Inputs/outputs	Value			Units	Test conditions
			Min.	Typ.	Max.		
High-level input voltage	V_{IH}	All inputs	2.0			V	
Low-level input voltage	V_{IL}	All inputs			0.8	V	
High-level output voltage	V_{OH}	All outputs	2.7			V	-60μA
Low-level output voltage	V_{OL}	All outputs except I_0 - I_4			0.5	V	0.8mA
High-level input current	I_{IH}	All inputs			50	μA	V_{IN} = 5.25V 25° C
Low-level output voltage	V_{OL1}	Outputs I_0 - I_4			0.4	V	3mA
High-level output current	I_{OH}	All outputs	60			μA	V_{OH} = 2.7V
Low-level output current	I_{OL0}	All outputs except I_0 - I_4	0.8			mA	V_{OH} = 0.5V
Low-level output current	I_{OL1}	Outputs I_0 - I_4	3.0			mA	V_{OL} = 0.4V
Input capacitance	C_{IN}	All inputs			10	pF	1MHz 100mV
Supply current	I_{CC}			50	80	mA	

AC CHARACTERISTICS

Characteristics	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
D_{OUT}	t_{pd1}			100	ns	Fig. 4 for loading; measure from CKE leading edge. See Fig. 5 for definition.
TP1	t_{pd2}			150	ns	Fig. 3 for loading; measure from CR and CKL. See Fig. 5 for definition.
TP2	t_{pd3}			150	ns	Fig. 3 for loading; measure from CKL trailing edge. See Fig. 5 for definition.
Propagation delays						
I_0 - I_4	t_{pd4}			200	ns	Fig. 4 for loading: measure from CR trailing edge.
Required delay from D_{IN} transition to CKL leading edge	t_1	50		430	ns	
Required delay from FAT + MIR transition to CKL leading edge	t_2	50		430	ns	
Required delay from CS transition to CKL trailing edge	t_3	50		430	ns	

CIRCUIT DIAGRAM

The line timing circuit consists of a 9-bit counter clocked by CKL and preset by PR. Counter states are decoded to form slip commands for the slip control logic and enable signals for the data inserter. The counter also controls the switching logic that delivers the write signals for the two elastic stores, i.e. channel and address, and the guard signals for the slip control circuit.

The channel elastic store has the function of retiming the 32 channels from D_{IN}, clocked by CKL, to D_{OUT} clocked by the exchange clock CKE. The address elastic store has the function of retiming the address of the 32 channels from the line clock CKL to parallel I_0 to I_4 outputs clocked by the exchange clock CKE.

The elastic stores are controlled by a slip control logic, which compares guard signals and the read reference signal. The read reference is generated together with 4 read signals from a 2-bit counter, driven by CR, in the exchange timing circuit. When the store capacity is about to be exceeded the slip control logic becomes active. The effects are a repetition (or jump) of channel zero for the two consecutive frames. Full capacity is always recovered after a normal slip. The contents of all other channels are unchanged during a slip.

A slip may also be forced in the presence of signal EN. This effect is a repetition (or jump) of channel 0 and address 0 for one frame only.

The data inserter modifies channel 0 data out according to Table 1:

Position	1	2	3	4	5	6	7	8
Frame TA	X	X	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6
Frame TB	X	1	Y_7	SL	X	X	X	X

Table 1 TSO format

Where SL is generated by the slip control logic Y_1 to Y_7 are external inputs and X indicates transparency through the circuit.

The circuit also has a master reset (MR) input for initialization of slip control and exchange timing circuits. TP1 and TP2 are also available as test points.

All inputs and outputs are compatible with LSTTL. Outputs I_0 - I_4 are capable of sinking 3mA at 0.4V.

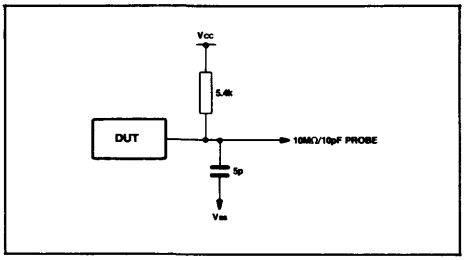


Fig.3

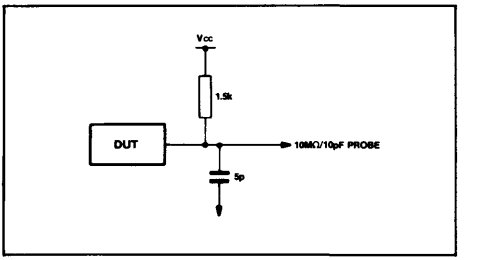


Fig.4

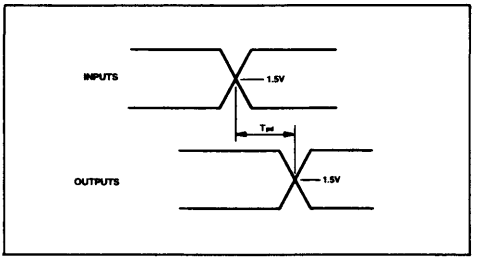


Fig.5 Waveforms for t_{pd}

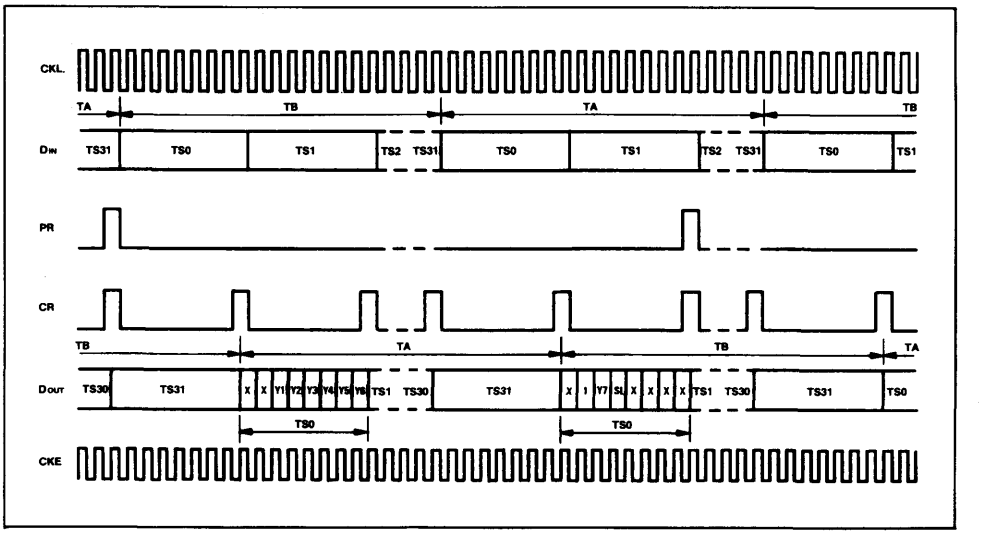


Fig.6 Timing diagram

PLESSEY
Semiconductors

MJ2812, MJ2812M 32 WORDS x 8 BIT FIFO MEMORY
MJ2813, MJ2813M 32 WORDS x 9 BIT FIFO MEMORY

The MJ2812 and MJ2813 are 32-word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three state outputs controlled by an output enable pin (OE). Data on the data inputs (D_0 – D_7) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs (Q_0 – Q_7) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal (IR) indicates that the device is ready to accept data and also provides a memory full signal.

Both the MJ2812 and MJ2813 have master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the D_0 input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the Q7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, IR, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

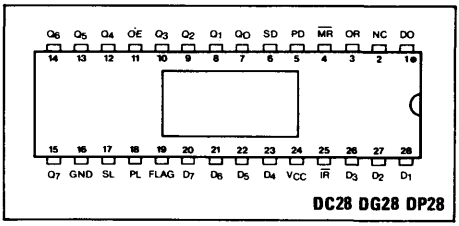


Fig. 1 MJ2812 (32 x 8) pin connections

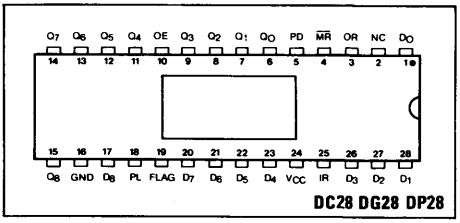


Fig. 2 MJ2813 (32 x 9) pin connections

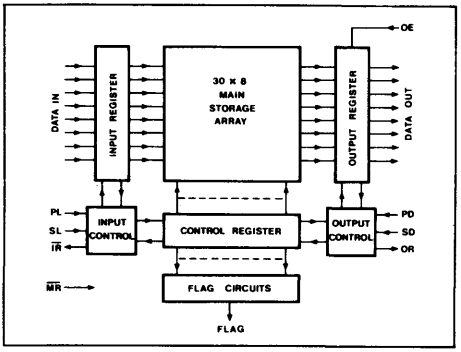


Fig. 3 MJ2812 simplified block diagram

FEATURES

- Serial or Parallel Inputs and Outputs (MJ2812 only)
- 32 Words x 8 Bits (MJ2812) and 32 Words x 9 Bits (MJ2813)
- Easily Stacked – Sideways or Lengthways
- Independent Reading and Writing
- Half-Full FLAG
- Data Rates up to 2.0 Mhz
- TTL – Compatible Tri-state Outputs
- Input and Output Ready Signals
- Master Reset
- Single +5V Supply

APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer Between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream, and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer-to-Line Printer Buffer

OPERATING RANGE

Type number	Ambient temperature	V_{CC}	Ground
MJ2812/MJ2813	0°C to +70°C	5.0V ±5%	0V
MJ2812M/MJ2813M	−55°C to +125°C	5.0V ±5%	0V

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
As specified in Operating Range table (above)

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Output high voltage	V_{OH}	2.4			V	$I_{OH} = -0.3mA$
Output low voltage	V_{OL}			0.4	V	$I_{OL} = 1.6mA$
Input high voltage	V_{IH}	2.5			V	
Input low voltage	V_{IL}			0.8	V	
Input leakage current	V_{IL}			10	µA	$V_{IN} = 0V$
Input high current	V_{IH}			10	µA	$V_{IN} = 5.25V$
V_{CC} current	I_{CC}		70	114	mA	$T_A = 0°C$ to $+70°C$
			70	120	mA	$T_A = -55°C$ to $+125°C$

Switching Characteristics

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Maximum parallel load or dump frequency	f_p	2812/3	2.05			Mhz	
		2812M/3M	1.5			MHz	
Delay, PL or SL high to IR inactive	t_{IR+}	2812/3	25	90	200	ns	
		2812M/3M	20	90	250	ns	
Delay, PL or SL low to IR active	t_{IR-}	2812/3	60	140	350	ns	
		2812M/3M	55	140	400	ns	
Minimum PL or PD high time	$t_{pwH(P)}$	All			80	ns	
Minimum PL or PD low time	$t_{pwL(P)}$	All			100	ns	
Minimum SL or SD high time	$t_{pwH(S)}$	All			80	ns	
Minimum SL or SD low time	$t_{pwl(S)}$	All			80	ns	
Data hold time	$t_{h(D)}$	All		130	200	ns	
Data set-up time	$t_{s(D)}$	All			0	ns	to PL
		All			0	ns	to SL
Delay, PD or SD high to OR low	t_{OR+}	2812/3	45	110	240	ns	OE high
		2812M/3M	40	110	260	ns	OE high
Delay, PD or SD low to OR high	t_{OR-}	2812/3	64	180	400	ns	DE high
		2812M/3M	60	180	400	ns	DE high
Ripple through time	t_{PT}	2812/3	0.4	1.0	2.5	µs	FIFO empty
		2812M/3M	0.4	1.0	3.0	µs	FIFO empty
Delay, OR low to data out changing	t_{DH}	All	35	90		ns	PD=low
Delay, data out to OR high	t_{DA}	All	0	70		ns	PD=high
Minimum reset pulse width	t_{MRW}	2812/3			290	ns	
		2812M/3M			300	ns	
Delay, OE low to output off	t_{DO}	All			250	ns	
Delay, OE high to output active	t_{EO}	All			250	ns	
Delay from PL or SL low to FLAG high or PD or SD low to FLAG low	t_{DF}	All			1.0	µs	
Input capacitance	c_I	All			7	pF	

NOTES
1. IR is active high on MJ2813 and active low on MJ2812
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

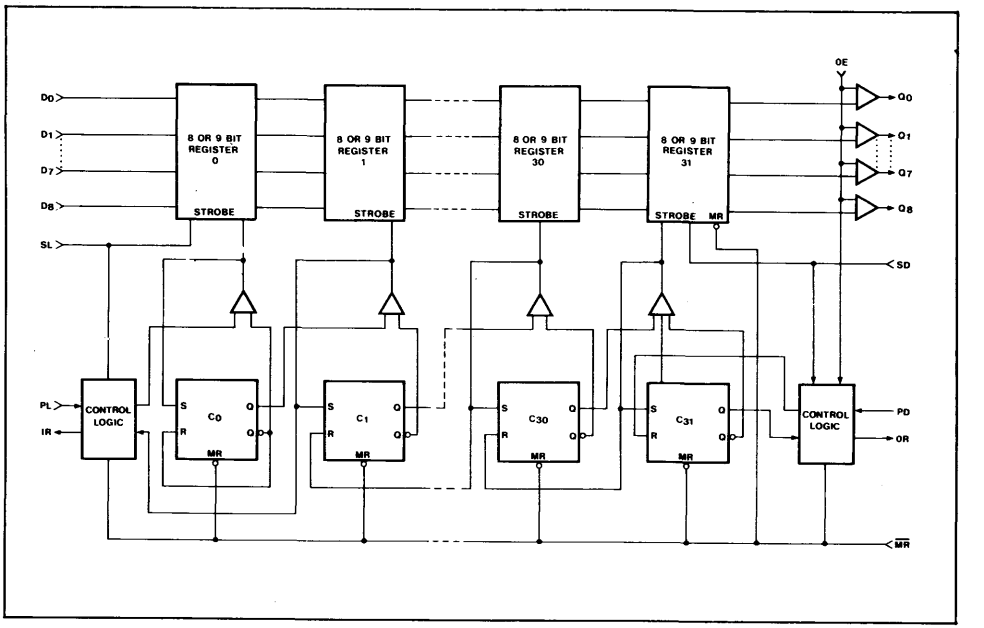


Fig. 4 Logic block diagram

MJ2812 AND MJ2813 FIFO OPERATION

The MJ2812 and MJ2813 FIFO's consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the (n)th data register, simultaneously setting the (n+1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused IR to go active, indicating the inputs are available for another data word.

Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the IR output signals).

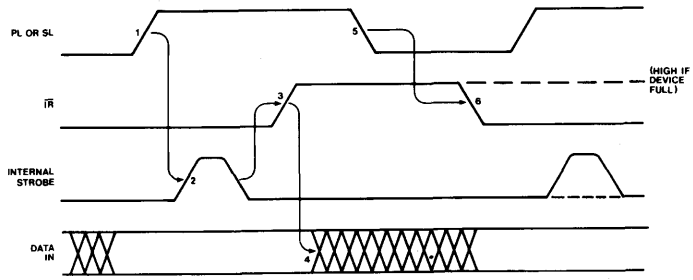
The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register than 'bubbles' back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

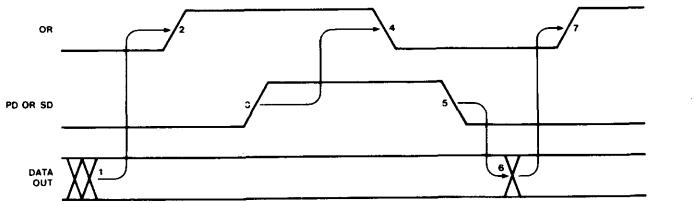
ABSOLUTE MAXIMUM RATINGS

Storage temperature	−65°C to +150°C
Temperature (ambient) under bias	−55°C to +125°C
Voltage on any pin w.r.t. ground (0V)	−0.3V to +9V
DC input voltage	−0.3V to +6V



MJ2812 INPUT TIMING

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.



MJ2812 OUTPUT TIMING

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The MJ2813 pattern is similar, but IR is active high instead of active low.

Fig. 5 MJ2812 timing diagram

Because the input ready signal is active low on the MJ2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812's fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812s connected end-to-end store 31n+1 words (instead of 32n). The MJ2813 stores 32n words in this configuration, because IR is active high and does dump the last word written into the second device.

Flag Output

A flag output is available on the MJ2812 and MJ2813 to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1μs of the 14th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1μs of the 20th PD or 160th SD high-low transition, ie. when 13 words remain in the memory.

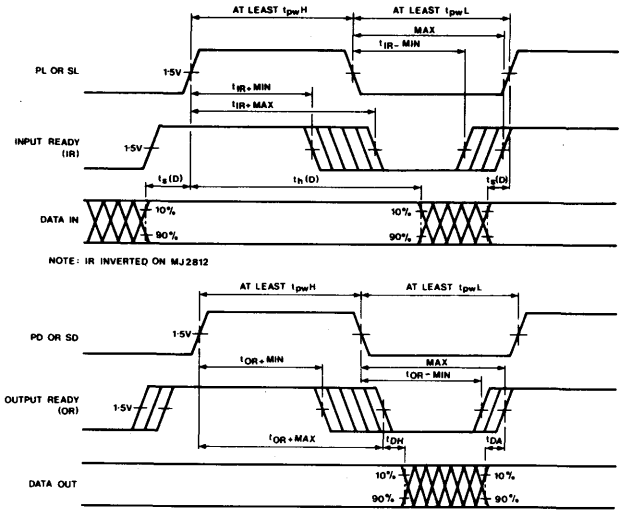
Serial Input and Output (MJ2812 Only)

The MJ2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to D_0 input.

The SL signal operates just like the PL input, causing IR to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, IR will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the Q_7 output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig. 6 Timing diagram

OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.

2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.

3. If PD is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least t_{OR+}) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.

4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.

5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.

6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.

7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.

PLESSEY
Semiconductors

MJ2841

64-WORD x 4-BIT FIRST-IN FIRST-OUT SERIAL MEMORY

The MJ2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four bit parallel word D_0-D_3 under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs Q_0-Q_3. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written.

A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFO's be placed side by side. Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.

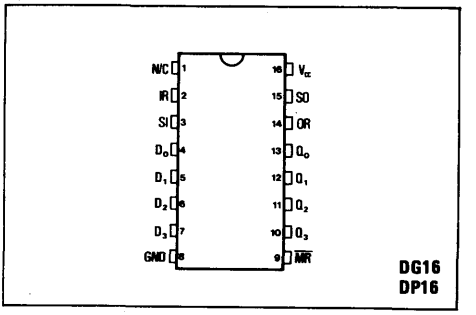


Fig.1 Pin connections (top view)

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +125°C
Ambient operating temperature	−10°C to +85°C
Lead temperature (soldering, 10s max.)	330°C
Voltage on any pin with respect to ground	−0.3V to +7V

FEATURES

- Single 5V Supply
- 1.75 MHz Guaranteed Data Rate (Typically 4 MHz)
- Pin Compatible with AM2841/Fairchild 3341
- Asynchronous Buffer For Up To 64 Four Bit Words
- Easily Expandable To Larger Buffers

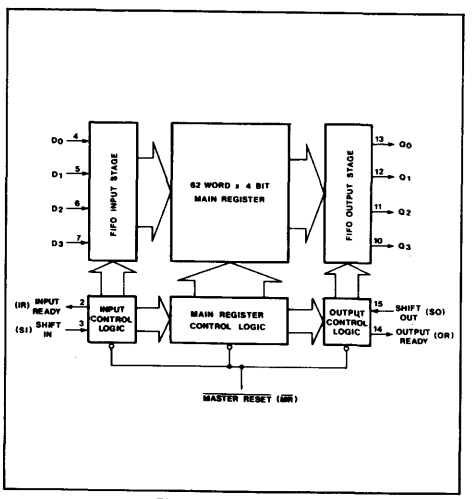


Fig.2 Block diagram

MJ2841 FIFO OPERATION

The MJ2841 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the n^{th} bit of control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the n^{th} data register, simultaneously setting the (n+1)th control register bit, so that the control flag moves with the data. In this fashion, data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs D_0-D_3 by applying a low to high transition on the shift in (SI) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes low indicating that data has been entered into the first data register and

the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the first control register bit is cleared. This causes IR to go high indicating the inputs are available for another data word.

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the four data outputs Q_0-Q_3. An input signal, shift out (SO) is used to shift the data out of the FIFO. A low to high transition on SO clears the last register bit, causing OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the '0' which is now present at the last register allows the data in the next to last register position to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back towards the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes high, OR will go low as before, but when SO next goes low, there is no data to move into the last location so OR remains low until more data arrives at the output. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all low).

ELECTRICAL CHARACTERISTICS

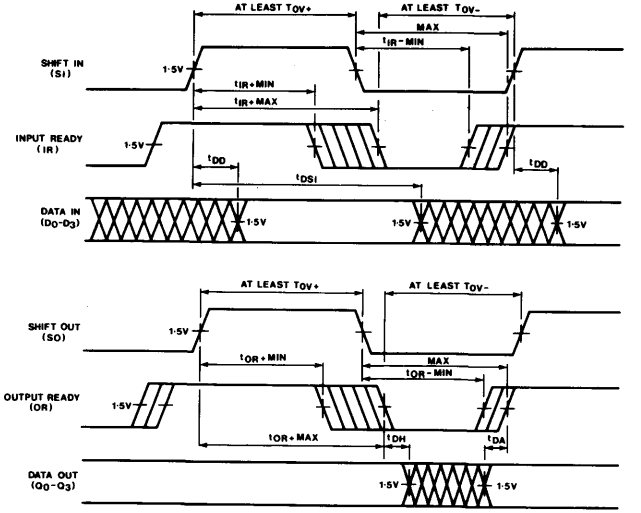
Test conditions (unless otherwise stated):
Supply voltage (V_{CC}) = +5V ±5%, T_{amb} = 0°C to +70°C
Typical Values at V_{CC} = 5V and T_{amb} = +25°C
All voltages with respect to ground

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
O/P high voltage	V_{OH}	2.7	3.2		V	I_{OH} = -0.2mA
O/P low voltage	V_{OL}		0.2	0.5	V	I_{OL} = 2mA
I/P high level	V_{IH}	2.5			V	
I/P low level	V_{IL}			0.8	V	
I/P leakage current	I_{IL}	-5		+10	μA	V_{IN} = 0V or 5V
Supply current	I_{CC}		50	81	mA	

Switching Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. SI or SO frequency	f_{MAX}	1.75	4.4		MHz	
Delay, SI high to IR low	$t_{IR}+$		50	120	ns	
Delay, SI low to IR high	$t_{IR}-$		80	200	ns	
Min. time SI and IR both high	$t_{OV}+$		<25	45	ns	
Min. time SI and IR both low	$t_{OV}-$		<25	45	ns	
Data release time	t_{DSI}		45	110	ns	
Data set-up time	t_{DD}		45	110	ns	
Delay, SO high to OR low	$t_{OR}+$		80	190	ns	
Delay, SO low to OR high	$t_{OR}-$		120	290	ns	
Ripple through time	t_{PT}		2.5	7	μs	FIFO empty
Delay, OR low to data out	t_{DH}	50	85		ns	SO = low
Min. reset pulse width	t_{MRW}		20	50	ns	
Delay, data out to OR high	t_{DA}	0	35		ns	SO = high
Input capacitance	CI			7	pF	Any pin



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DONT CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN

Fig.3 Timing diagram

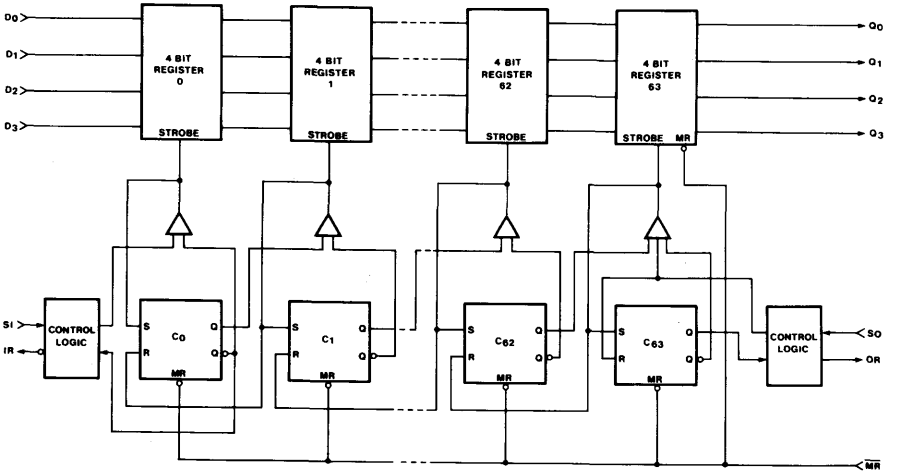


Fig.4 Logic block diagram

OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However OR will remain low, indicating data at the output is not valid.
2. When the output data changes as a result of a pulse on SO, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.
3. If SO is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR}+$) and then will go back to low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought low.
4. When the master reset is brought low, the control register and the outputs are cleared. IR goes high and OR goes low. If SI is high when the master reset goes high then the data on the inputs will be written into the memory and IR will return to the low state until SI is brought low. If SI is low when the master reset is ended, the IR will go high, but the data on the inputs will not enter the memory until SI goes high.

PLESSEY Semiconductors — PRELIMINARY INFORMATION CMOS

MV3506 EXP A-LAW CODEC WITH FILTER
MV3507 EXP μ-LAW CODEC WITH FILTER
MV3507A EXP μ-LAW CODEC WITH FILTER AND A/B SIGNALLING

The MV3506 and MV3507 are silicon gate CMOS Companding Encoder/Decoder integrated circuits designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analogue to digital conversion circuits that conform to the desired transfer characteristic. The MV3506 provides the European A-Law companding and the MV3507 provides the North American μ-Law companding characteristic.

These circuits provide the interface between the analogue signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operates from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or asynchronous operation.

In 22-pin packages (0.400in centres) the MV3506/MV3507 are ideally suited for PCM applications: Exchange, PABX, Channel Bank or Digital Telephone as well as fibre optic and other non-telephone uses. A 28 pin version, the MV3507A, provides standard μ-Law A/B signalling capability.

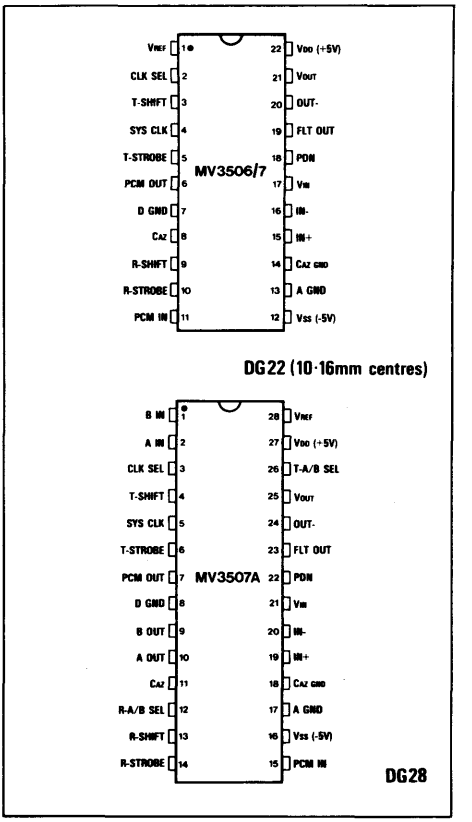


Fig.1 Pin connections - top view

FEATURES

- Independent Transmit and Receive Sections with 75dB Isolation
- Low power CMOS 80mW (Operating) 10mW (Standby)
- Stable Voltage Reference On-chip
- Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- Input Analogue Filter Eliminates Need for External Anti-aliasing Prefilter
- Input/Output Op. Amps for Programming Gain
- Output Op. Amp Provides ±3.1V Into a 1200 Ohms load or Can Be Switched Off for Reduced Power (70mW)
- Special Idle Channel Noise Reduction Circuitry
- Encoder has Dual-speed Auto-zero Loop for Fast Acquisition on Power-up
- Low Absolute Group Delay = 410μsec. at 1kHz

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{DD}: +6.0V
DC Supply Voltage V_{SS}: -6.0V
Operating Temperature: -25°C to +70°C
Storage Temperature: -65°C to +150°C
Power Dissipation at 25°C: 1000mW
Digital Input: V_{SS} -0.3≤V_{IN}≤V_{DD} -0.3
Analogue Input: V_{SS} -0.3≤V_{IN}≤V_{DD} -0.3

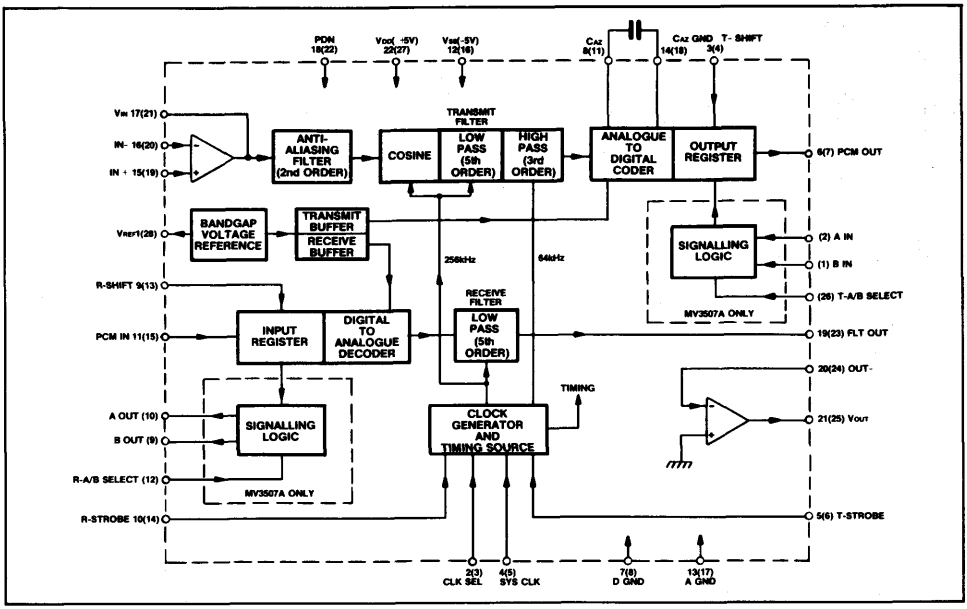


Fig.2 MV3506/MV3507/MV3507A block diagram. Pin numbers for the MV3507A are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C

Power Supply Requirements

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply	V_{DD}	4.75	5.0	5.25	V	
Negative supply	V_{SS}	-4.75	-5.0	-5.25	V	
Power dissipation (operating)	P_{OPR}		80	110	mW	V_{DD} = 5.0V, V_{SS} = -5.0V
Power dissipation (operating w/o output op. amp	P_{OPR}		70		mW	
Power dissipation (standby)	P_{STBY}		10	20	mW	

AC Characteristics (see Fig. 6)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
System clock duty cycle	D_{SYS}	40	50	60	%	At 1.544MHz or 2.048MHz
Shift clock frequency	f_{SC}	0.064		2.048	MHz	
Shift clock duty cycle	D_{SC}	40	50	60	%	
Shift clock rise time	t_{rc}			100	ns	
Shift clock fall time	t_{fc}			100	ns	
Strobe rise time	t_{rs}			100	ns	
Strobe fall time	t_{fs}			100	ns	
Shift clock to strobe (On) delay	t_{sc}	-100	0	200	ns	
Strobe width	t_{sw}	600ns		124.3μs		At 2.048MHz,700ns min at 1.544MHz
Shift clock to PCM out delay	t_{cd}		100	150	ns	
Shift clock to PCM in set-up time	t_{dc}	60			ns	
PCM output rise time C_L = 100pF	t_{rd}		50	100	ns	To 3V;510Ω to V_{DD}
PCM output fall time C_L = 100pF	t_{fd}		50	100	ns	To 0.4V;510Ω to V_{DD}
A/B select to strobe trailing edge	t_{dss}	100			ns	

DC Characteristics at V_{DD} = +5V, V_{SS} = -5V, V_{ref} = -3.075V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analogue input resistance	R_{INA}	100			kΩ	
Input capacitance	C_{IN}		7	15	pF	All logic and analogue inputs
Logic input low current (Shift clock, PCM IN, System clock)	I_{INL}			1	μA	V_{IL} = 0.8V
Logic input high current	I_{INH}			1	μA	V_{IH} = 2.0V
Logic input low current (Strobe, A/B Sel, A IN B IN, PDN)	I_{INL}			600	μA	V_{IL} = 0.8V
Logic input high current	I_{INH}			600	μA	V_{IH} = 2.0V
Logic input 'low' voltage	V_{IL}			0.8	V	
Logic input 'high' voltage	V_{IH}	2.0			V	
Logic output 'low' voltage (PCM out)	V_{OL}			0.4	V	510Ω pull-up to V_{DD} + 2 LS TTL
Logic output 'low' voltage (A/B out)	V_{OL}			0.4	V	I_{OL} = 1.6mA
Logic output 'high' voltage	V_{OH}	2.6			V	I_{OH} = 40μA
Output load resistance V_{OUT}	R_L	1200			Ω	C_L = 50pF max.

Transmission Delays

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Encoder			125		μs	From T_{STROBE} to the start of digital transmitting
Decoder		30	8T+25		μs	T = Period in μs of R_{SHIFT} CLOCK
Transmit section filter				182	μs	At 1kHz
Receive section filter				110	μs	At 1kHz

MV3506 Single-Chip A-Law Filter/Codec Linear Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Idle channel noise (weighted noise)	ICN_W		-85	-73	dBm0p	CCITT G.712 5.1
Idle channel noise (single frequency noise)	ICN_{SF}			-60	dBm0	CCITT G.712 5.2
Idle channel noise (receive section)	ICN_R			-28	dBm0p	CCITT G.712 5.3
Spurious out-of-band signals at the channel output				-30	dBm0	CCITT G.712 7.1
Intermodulation (2 tone method)	IMD_{2F}			-35	dBm0	CCITT G.712 8.1
Intermodulation (1 tone + power frequency)	IMD_{PF}			-49	dBm0	CCITT G.712 8.2
Spurious in-band signals at the channel output port				-40	dBm0	CCITT G.712 10
Inter-channel crosstalk $V_{IN-VOUT}$		75	80		dB	CCITT G.712 12
Max.coding analogue input level	$V_{IN}(max)$		±3.1		V_{0pk}	
Max.coding analogue output level	$V_{OUT}(max)$		±3.1		V_{0pk}	R_L = 1.2kΩ
Gain variation with temperature and power supply	ΔG		±0.25		dB	
Transmit gain repeatability			±0.1	±0.2	dB	
Receive gain repeatability			±0.1	±0.2	dB	
Zero transmission level point (decoder) (see Fig. 3)	$0TLP_R$		+5.8		dBm	V_{OUT} digital milliwatt response
Zero transmission level point (encoder)	$0TLP_T$		+5.8		dBm	V_{IN} to yield same as digital milliwatt response at decoder

MV350(7)A Single-Chip μ-Law Filter/Codec Linear Characteristics

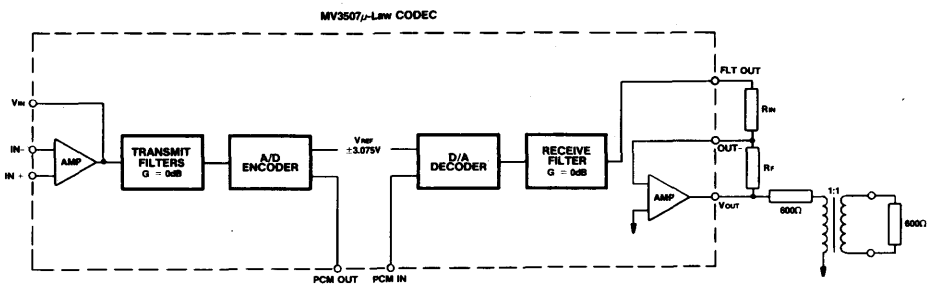
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Idle channel noise (weighted noise)	ICN_W		5	17	dBrnc0	CCITT G.712 5.1
Idle channel noise (single frequency noise)	ICN_{SF}			-60	dBm0	CCITT G.712 5.2
Idle channel noise (receive section)	ICN_R			15	dBrnc0	CCITT G.712 5.3
Spurious out-of-band signals at the channel output				-28	dBm0	CCITT G.712 7.1
Intermodulation (2 tone method)	IMD_{2F}			-35	dBm0	CCITT G.712 8.1
Intermodulation (1 tone + power frequency)	IMD_{PF}			-49	dBm0	CCITT G.712 8.2
Spurious in-band signals at the channel output port				-40	dBm0	CCITT G.712 10
Inter-channel crosstalk V_{IN}-V_{OUT}		75	80		dB	CCITT G.712 12
Max.coding analogue input level	$V_{IN}(max)$		±3.1		V_{0pk}	
Max.coding analogue output level	$V_{OUT}(max)$		±3.1		V_{0pk}	$R_L = 1.2k\Omega$
Gain variation with temperature and power supply	ΔG		±0.25		dB	
Transmit gain repeatability			±0.1	±0.2	dB	
Receive gain repeatability			±0.1	±0.2	dB	
Zero transmission level point (decoder) (see Fig. 3)	$0TLP_R$		+5.8		dBm	V_{OUT} Digital milliwatt response
Zero transmission level point (encoder)	$0TLP_T$		+5.8		dBm	V_{IN} to yield same as digital milliwatt response at decoder

PIN/FUNCTION DESCRIPTIONS

Name	Pin		Description
	MV3506/ MV3507	MV3507A	
SYS CLK	4	5	**System Clock** This pin is a TTL compatible input for either a 1.544MHz or a 2.048MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock** This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock** This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe** This TTL compatible pulse input (8kHz) is used for analogue sampling and for initiating the PCM output from the coder. It must be synchronised with the T-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
P-STROBE	10	14	**Receive Strobe** This TTL compatible pulse input (typ. 8kHz) initiates clocking of PCM input data into the decoder. It must be synchronised with the R-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select** This pin selects the proper divide ratios to utilise either 1.544MHz or 2.048MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz and to V_{SS} (-5V) for 1.544MHz operation. If this pin is connected to DGND, 256kHz may be used as the system clock.
PCM OUT	6	7	**PCM Output** This is a LS TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of T-SHIFT clock signal following a positive edge on the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS TTL inputs.
PCM IN	11	15	**PCM Input** This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.

PIN/FUNCTION DESCRIPTIONS

Name	Pin		Description
	MV3506/ MV3507	MV3507A	
C_{AZ}	8	11	**Auto Zero Capacitor** A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation.
C_{AZ}GND	14	18	Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{REF}	1	28	Output of the internal **Band-gap Reference Voltage** (-3.075V) generator is brought out to V_{REF} pin.
IN +	15	19	**Analogue input.** IN- and IN + are the inputs of a high input impedance op. amp and V_{IN} is the output of this op. amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain of as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. channel.
IN-	16	20	
V_{IN}	17	21	
FLT OUT	19	23	**Filter Out** This is the output of the low pass filter which represents the recreated analogue signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 20kΩ.
OUT-	20	24	**Output and input of the uncommitted output amplifier stage.** Signal at the FLT OUT pin can be connected to this amplifier to realise a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into 600Ω load. (See Fig. 3.) If OUT- is connected directly to V_{SS} the op. amp will be powered down, reducing power consumption by 12mW, typically.
V_{OUT}	21	25	
V_{DD}	22	27	**Power supply pins.** V_{DD} and V_{SS} are positive and negative supply pins, respectively (typ. +5V, -5V).
V_{SS}	12	16	
A GND	13	17	**Analogue and Digital Ground pins** are separate for minimising crosstalk and digital interference.
D GND	7	8	
PDN	18	22	**Power Down** This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
A IN		2	The **Transmit A/B select** input (T-A/B SEL) selects the **A signal** input in a positive transition and the **B signal** input on the negative transition. These inputs are TTL compatible. The A/B signalling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronised to the T-STROBE input in each device.
B IN		1	
T-A/B SEL		26	
A OUT		10	In the decoder the A/B signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which the **Receive A/B select (R-A/B SEL)** input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.
B OUT		9	
R-A/B SEL		12	



$$OTLP_{IN} = -\left[G - 20 \log \left(\frac{V_{REF}}{1.58}\right)\right]$$

$$= -\left[0 - 20 \log \left(\frac{3.075}{1.58}\right)\right]$$

$$= +5.8\text{dBm at the } V_{IN} \text{ terminal}$$

$$OTLP_{OUT} = \left[G + 20 \log \left(\frac{V_{REF}}{1.58}\right)\right]$$

$$= \left[0 + 20 \log \left(\frac{3.075}{1.58}\right)\right]$$

$$= +5.8\text{dBm at the } FLT_{OUT} \text{ terminal}$$

(Note: The 1.58V value is that value of reference voltage that would allow the peak value of +3.17dBm as the maximum coded value, resulting in a OTLP of 0dBm. For A-Law it would be 1.57V for +3.14dBm.)

Since the output buffer amplifier is designed to drive 1200Ω, a 600Ω resistor in series with the 600Ω load divides the available voltage in half resulting in a $OTLP_{OUT}$ to the load of -0.2dBm.

For a system where OTLP is chosen to be 0dBm the input op. amp. should be configured for 5.8dB gain and the output op. amp. for 0.2dB gain. R_{IN} should be ≥20kΩ.

Fig.3 MV3507 and MV3507A μ-law Codec input/output reference signal levels

Power Down Logic

Powering down the Codec can be done in several ways. The most direct is to drive the PDN pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high, low or disconnected.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (-3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimise crosstalk. This reference voltage is trimmed to within ±27mV during assembly to ensure a minimum gain error of ±0.2dB due to all causes.

FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the MV3506/MV3507. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A band-gap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analogue signals first enter the chip at the uncommitted op. amp terminals. This op. amp allows gain trim to be used to set OTLP in the system. From the V_{IN} pin the signal enters the 2nd Order analogue anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typ) at 256kHz and 44dB (typ) at 512kHz. From the cosine filter the signal enters a 5th Order low-pass filter clocked at 256kHz, followed by a 3rd Order high-pass filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are 26dB (typ) from 0 to 60Hz and 35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analogue-to-digital conversion process requires 9 1/2 clock cycles, or about 72μs. The 8 bit PCM date is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

Included in the circuitry of the MV3507 is 'All Zero' code suppression so that negative input signal values between decision values numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronisation by TI line clock recovery circuitry as there are never more than 15 consecutive zeroes.

An additional feature of the Codec is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250ms the only code words generated were +0, -0, +1 or -1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation resetting the 250ms timer. This feature is a form of Idle Channel Noise 'Squelch' or 'Crosstalk Suppression'. It is of particular importance in the MV3506 A-Law version because the A-Law transfer characteristic has 'mid-riser' bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialised to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order low-pass filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalisation to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 20kΩ. When used in this fashion the low impedance output amp can be switched off for a considerable savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Fig. 3 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Timing Requirements

The internal design of the Single-Chip Codec paid careful attention to the timing requirements of various systems. In North America, central office and channel bank designs follow the American Telephone and Telegraph Company's *TI Carrier PCM format to multiplex 24 voice channels at a* data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Nevertheless, in digital telephone designs, Codec's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The MV3507 and MV3507A fulfil these requirements.

In Europe, telephone exchange and channel bank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The MV3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the Plessey Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the MV3506/MV3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+)edges of the strobe, forcing the PCM output in high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronised to it. Figures 4 and 5 show the waveforms in typical multiplexed uses of the Codec.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz or 1.544MHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be any frequency between 64kHz and 2.048MHz as long as one of the two system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous operation of transmit and receive.

Signalling In μ-Law Systems

The MV3506 and MV3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signalling information to be carried in the bit stream with the coded analogue data. This coding scheme is sometimes called 7 5/6 bit rather than 8 bit because of the LSB every 6th frame being replaced by a signalling bit. This is referred to as A/B Signalling and if a signalling frame carries the 'A' bit, then 6 frames later the LSB will carry the 'B' bit. To meet this requirement, the MV3507A is available in a 28-pin package, as 6 more pins are required for the inputs and outputs of the A/B signalling.

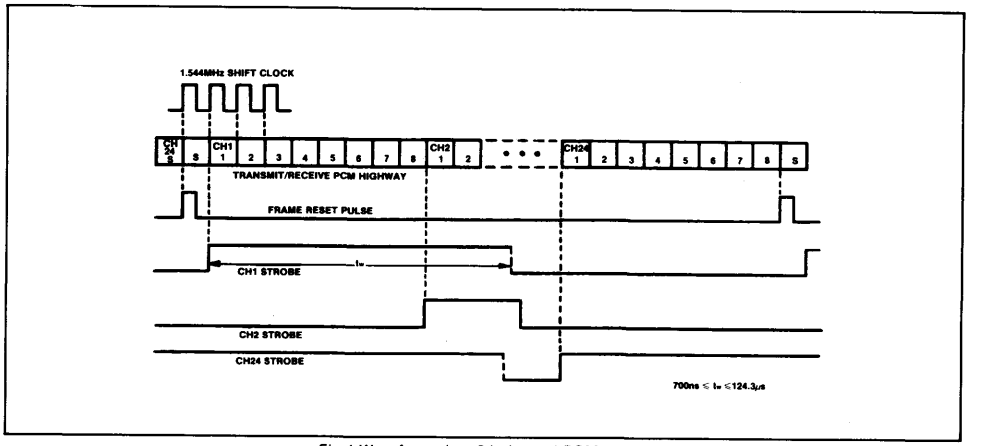


Fig.4 Waveforms in a 24 channel PCM system

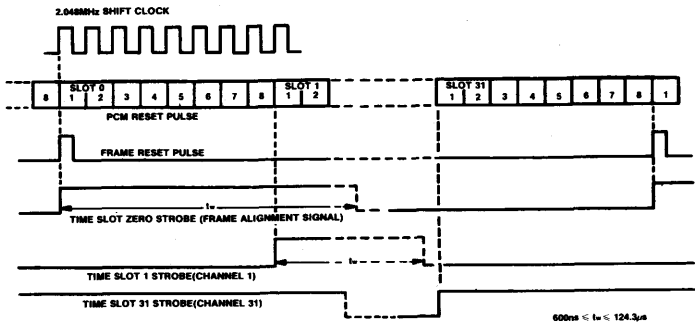
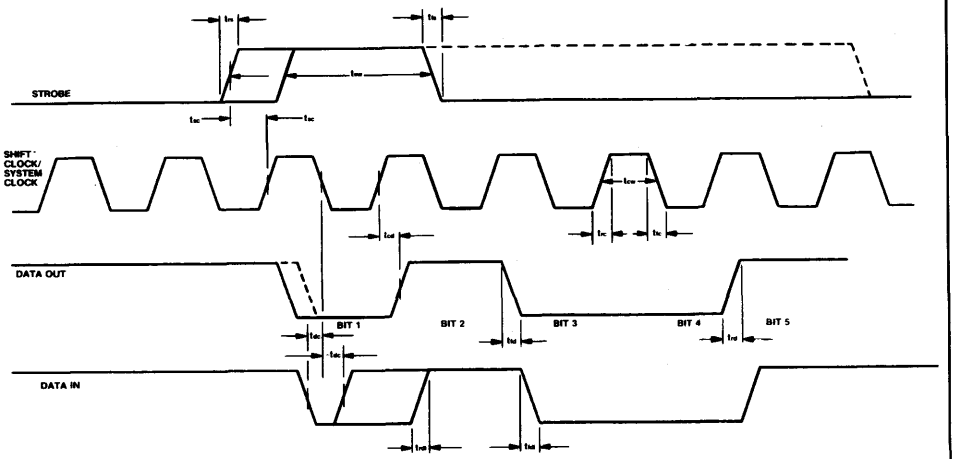


Fig.5 Waveforms in a 30 channel PCM system



*In this example the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same the relationship of each to the strobe remains the same. The system clock and shift clock need not have coincident edges, but must relate to the strobe within the t_{sc}, timing requirements.
The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.
The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

Fig.6 Waveform details

	Min.	Max.
t_{cw}	195nsec	9.38μsec
t_{rs}		100ns
t_{fs}		100ns
t_{sc}	-100ns	200ns **
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec
t_{cd}	100ns	150ns
t_{dc}	60ns	
t_{rdi}		100ns
t_{fdi}		100ns

*At 2.048MHz, 700ns at 1.544MHz
**That is, the strobe can produce the shift clock by 200ns, or follow it by as much as 100ns.

Signalling Interface

In the AT&T TI carrier PCM format an A/B signalling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signalling conditions (A and B) per channel, giving four possible signalling states per channel are repeated every 12 frames (1.5 milliseconds). The A signalling condition is sent in bit 8 of all 24 channels in frame 6. The B signalling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The MV3507A in a 28-pin package is designed to simplify the signalling interface. For example, the A/B select input pins are transition sensitive. The Transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronises the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channel bank. The A and B signalling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and negative in the beginning of frame 11 (see Fig. 7).

The decoder uses a similar scheme for receiving the A and B signalling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the Receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

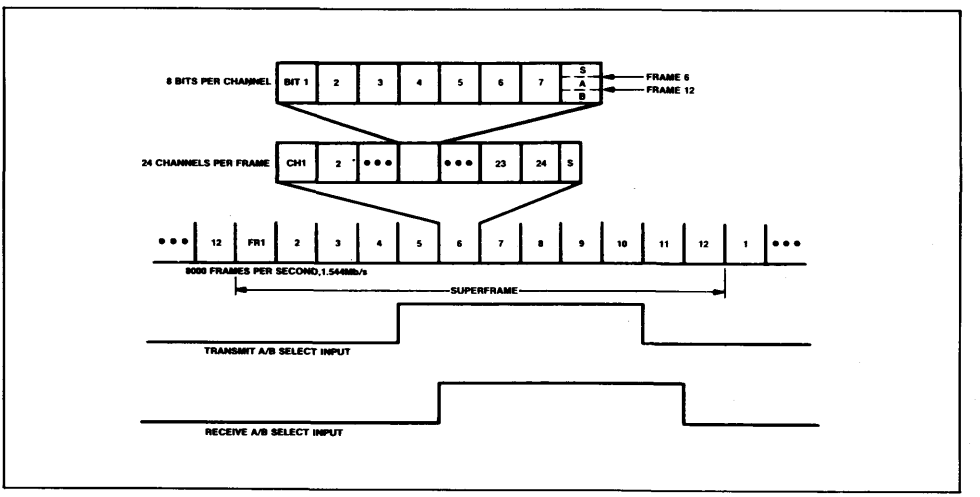


Fig.7 Signalling waveforms in a TI carrier system

In the TI carrier system, 24 voice channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s. Within the channel bank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for asynchronous operation. Asynchronous operation helps minimise switching delays through the system. Since the timing interface for the coder and decoder sections is independent of each other in the MV3507A, it can be operated in either manner.

In the CCITT carrier system 30 voice channels and 2 framing and signalling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channel bank can generate the timing signals for all channels. Generation of the timing signals for the MV3506 and MV3507A is straightforward because of the simplified timing requirements (see timing requirements for details). Figures 9 and 10 show design schemes for generating these timing signals in a common circuitry. Note that only three signals; a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channel bank. Since the Plessey Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

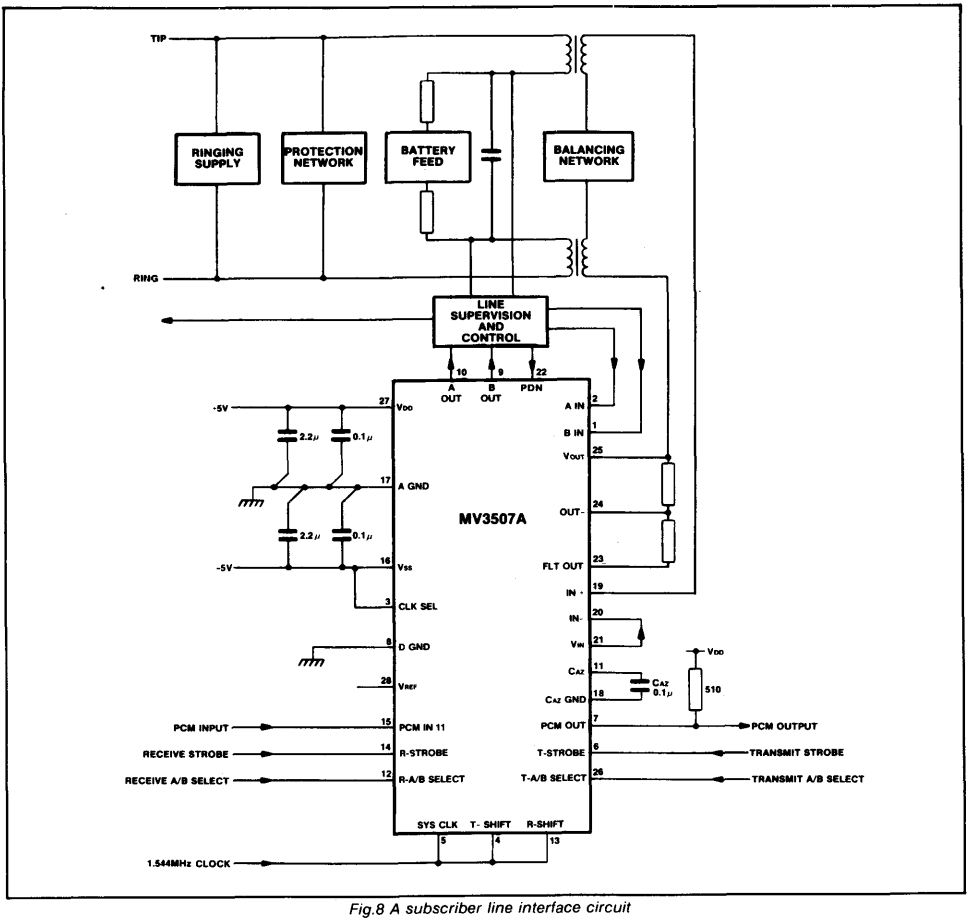


Fig.8 A subscriber line interface circuit

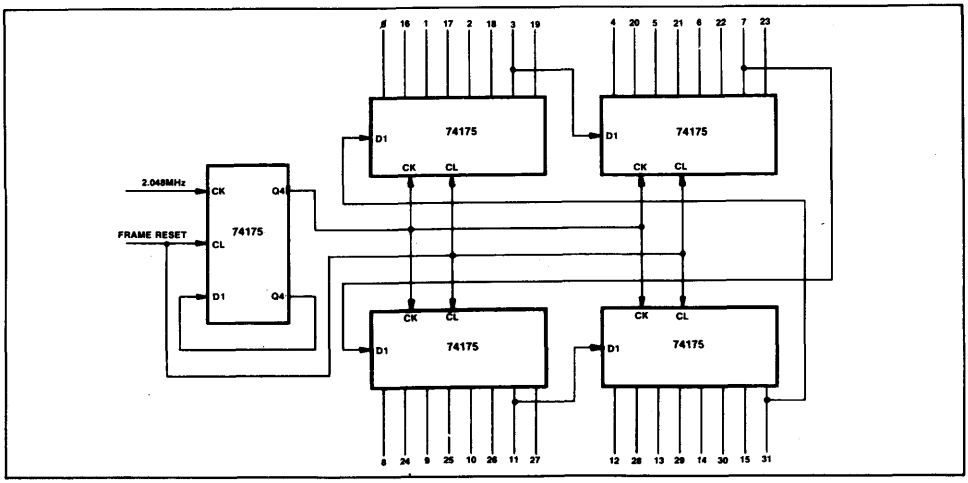


Fig.9 Generating timing signals in a CCITT carrier system (30 + 2 channels)

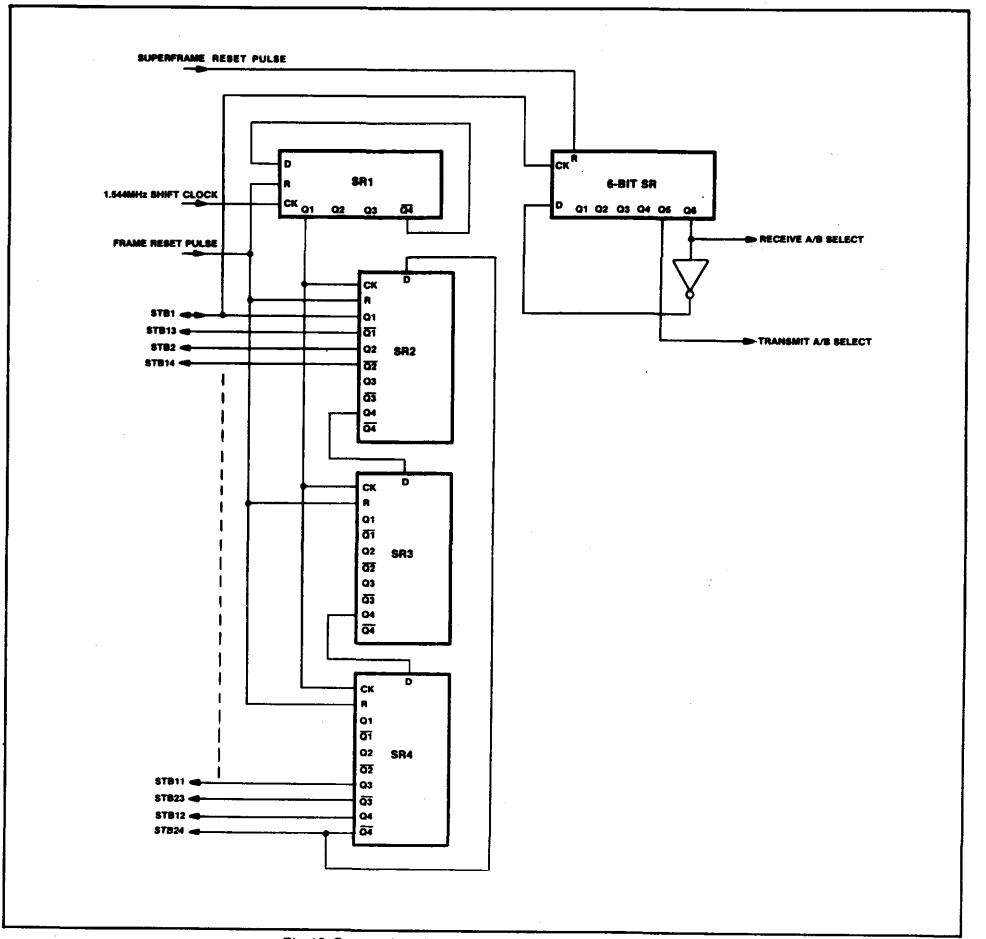


Fig.10 Generating timing signals in a TI carrier system

A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs of interface to the switch. Two pairs carry transmit and receive PCM voice date. One pair supplies an 8kHz synchronising clock signal and the remaining pair supplies power to the telephone. More sophisticated techniques minimise the number of wire pairs. The Plessey Single-Chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 11 shows a schematic for a typical digital telephone design.

Since asynchronous operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 2048kHz system clock and 64kHz shift clock from the 8kHz synchronising signal received from the switch. The synchronising signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output directly feeds into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

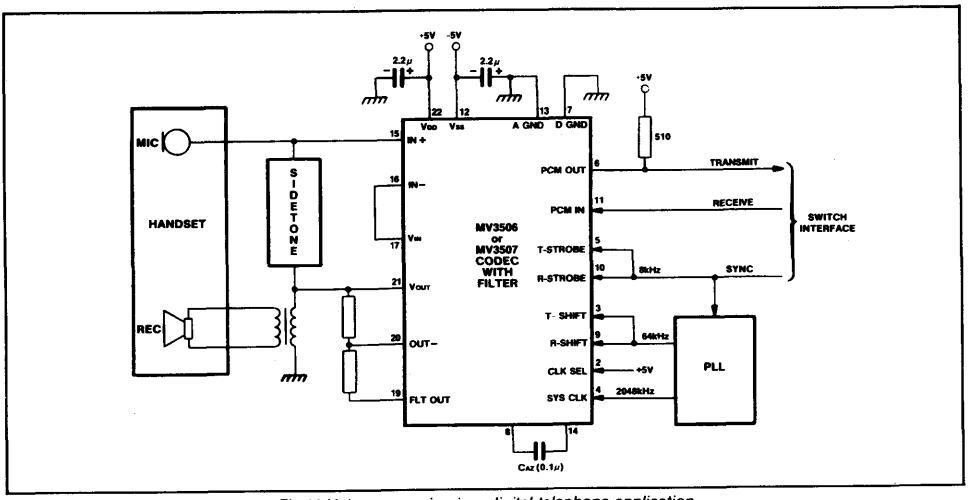


Fig.11 Voice processing in a digital telephone application

PLESSEY Semiconductors

ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV4320 MV4322 MV4323

KEYPAD PULSE DIALLER

The MV4320 series is fabricated using ISO-CMOS high density technology. The device is a pin-for-pin replacement for the DF320 Loop Disconnect Dialler and offers wider operating supply voltage range and lower power dissipation. The MV4320 accepts up to 20 digits from a standard 2 of 7 keypad and offers a REDIAL option activated by key #. The device provides dial pulsing and muting outputs and has a HOLD pin for interrupting a dialling sequence. Outpulsing mark/space ratio and dialling speed are pin selectable.

The MV4322 and MV4323 provide the same function as the MV4320, except the MV4322 provides the M2 muting function in place of M1 and the MV4323 provides "Inter Digit Pause" (IDP) selection in place of Mark/Space (M/S) ratio selection.

The MV4320, MV4322 and MV4323 are available in Ceramic DIL (DG, -40°C to +85°C).

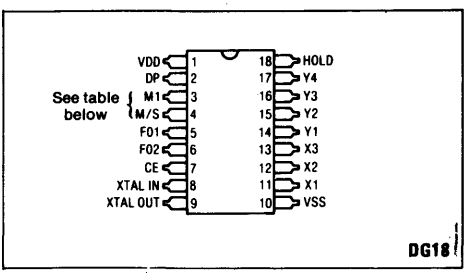


Fig.1 Pin connections (top view)

Type No.	Pin 3	Pin 4
MV4320	M1	M/S
MV4322	M2	M/S
MV4323	M1	IDP

FEATURES

- Pin for Pin Replacement for the DF320
- 2.5V to 5.5V Supply Voltage Operating Range
- 375μW Dynamic Power Dissipation at 3V
- Uses Inexpensive 3.58 MHz Ceramic Resonator or Crystal
- Stores up to 20 Digits
- Selectable Outpulsing Mark/Space Ratio
- Selectable Dialling Speeds of 10, 16, 20 and 32 Hz
- Low Cost

APPLICATIONS

- Pushbutton Telephones
- Tone to Pulse Converters
- Mobile Telephone
- Repertory Dialers

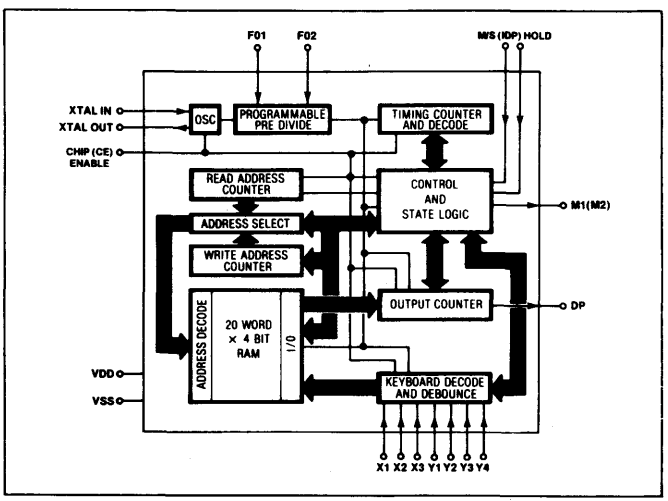


Fig.2 MV4320/MV4322/MV4323 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.5		5.5	V		
2		Standby Supply Current		I_{DDS}		1.0	10.0	µA	CE = V_{SS}	
3		Operating Supply Current		I_{DD}		125	200	µA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-8.0	µA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, IDP, F01,
7		Pull-Down Transistor Sink Current		I_{IH}	0.5*	3.0	8.0	µA	$V_{IN} = V_{DD}$	F02, FD, HOLD
8		Logic '0' Level		V_{IL}			0.9	V	All inputs	
9		Logic '1' Level		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel Sink	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M1/M2
13			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = 3.0V; T_{amb} = +25°C; f_{CLK} = 3.579545MHz
All voltages wrt V_{SS}

		CHARACTERISTICS	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
14	DYNAMIC	Output Rise Time	t_R		1.0		us	DP, M_1.
15		Output Fall Time	t_F		1.0		us	C_L = 50pF
16		Maximum Clock Frequency	t_{CLK}	3.58			MHz	3.579545 MHz Crystal
17		Mark to Space Ratio	M/S		2:1			Note 1
18					3:2			
19		Impulsing Rate = $\frac{1}{T}$			10		Hz	Note 1
20					16			
21					20			
22					932			
23		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE '1'
24		Input Capacitance	C_{in}		5.0		pF	Any Input

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

NOTES:
1. See Pin Function, Table 1.

OPERATING NOTES

The first key entered in any dialling sequence initiates the oscillator by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in figures 3 and 4. Figure 3 shows use of the circuits with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialler circuit. In this mode, the pulse occurring on M1 when CE is taken high, with no keypad input, can be used to initiate the bistable latching relay. Figure 4 shows the timing diagram for the CE internal control mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously.

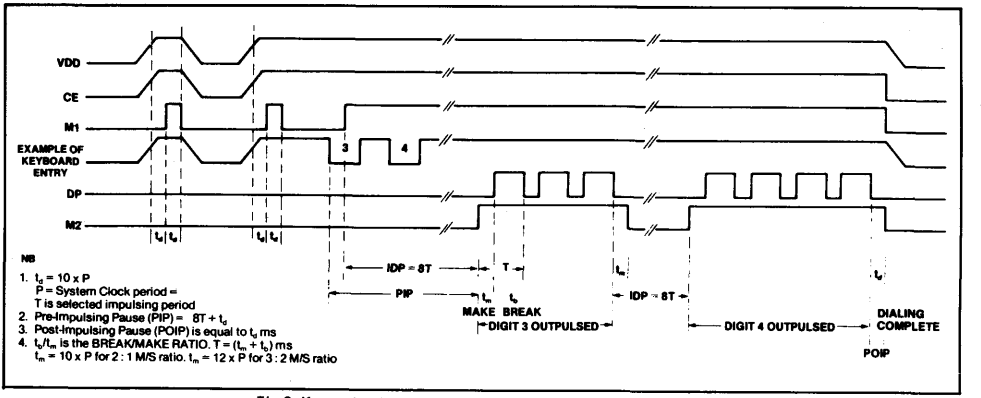


Fig.3 Keypad pulse dialer timing diagram, CE-External control

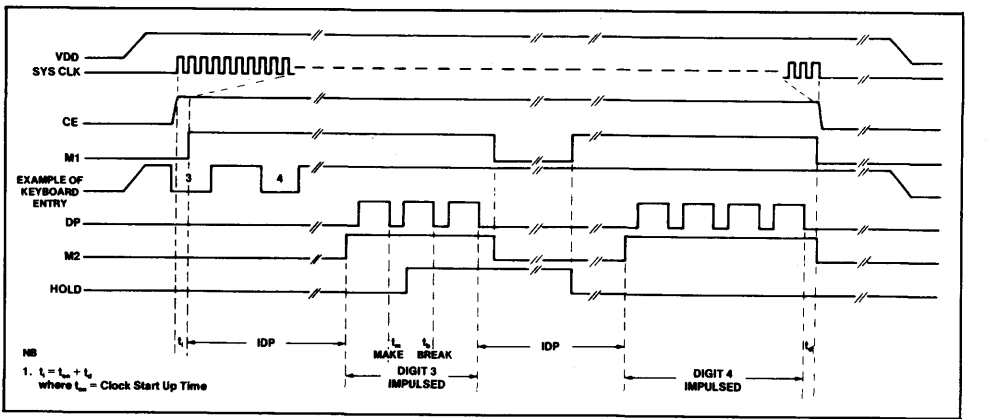


Fig.4 Keypad pulse dialer timing diagram, CE-Internal control

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN.	MAX.
V_{DD}-V_{SS}	-0.3V	10V
Voltage on any pin	V_{SS} -0.3V	V_{DD} +0.3V
Current at any pin		10mA
Operating Temperature	-40°C	+85°C
Storage Temperature	-65°C	+150°C
Power Dissipation		1000mW

Derate 16mW/°C above 75°C. All leads soldered to PC board.

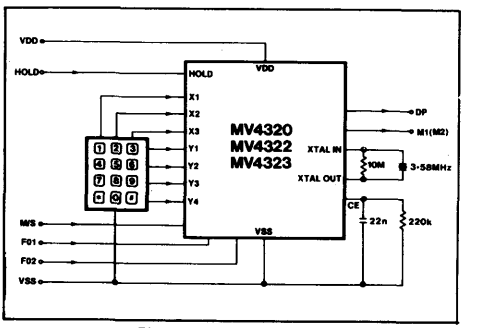


Fig.5 Application diagram

PIN FUNCTIONS

V_{DD}	Positive voltage supply					
DP	Dial Pulsing Output Buffer					
M1/M2	Mute Output (Off Normal) Buffer					
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}. Note: O/C = Open Circuit				O/C	2:1
					V_{DD}	3:2
IDP	Inter-Digit Pause Select. Note: T = Selected Impulsing Period				O/C	8T
					V_{DD}	4T
F01,F02	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}. * Assumes f_{CLK} = 3.579545MHz.	F01	F02	Nominal Impulsing Rate	Actual* Inpulsing Rate	System Clock frequency
		O/C	O/C	10Hz	10.13Hz	303.9Hz
		O/C	V_{DD}	20Hz	19.42Hz	582.6Hz
		V_{DD}	O/C	932Hz	932.17Hz	27,965.1Hz
		V_{DD}	V_{DD}	16Hz	15.54Hz	466.1Hz
CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.					
XTAL IN	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.					
XTAL OUT	Crystal Output Buffer to drive crystal.					
V_{SS}	System ground					
X_1,X_2,X_3	Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.					
Y_1,Y_2,Y_3,Y_4	Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.					
HOLD	Prevents further impulsing. On-chip pull-down transistor to V_{SS}.	O/C	Normal Operation			
		V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete			

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MV4325/MV4326/MV4327

PROGRAMMABLE KEYPAD PULSE DIALLER

The MV4325 Keypad Pulse Dialler contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The MV4325 has programmable access pause capability to provide automatic interruption of dialling needed when accessing the toll network, WATS line or public network. The device is fabricated using Plessey Semiconductors' ISO-CMOS technology which enables the device to function down to 2.0V making it ideal for long loop operation.

The MV4325 will accept up to 20 digits and access pauses and will redial stored information at a later time by activation of # key. Device current in standby is less than 1μA at 1.0V.

The MV4326 provides the same function as the MV4325 except that the M2 muting function is provided instead of M1 offered in the MV4325.

The MV4327 has both M1 and M2 muting functions but no KT output.

The MV4325 and MV4326 are available in Ceramic DIL (DG, −40°C to +85°C).

APPLICATIONS

- Pushbutton Telephones with Last Number Redial
- Repertory Dialers
- Tone to Pulse Converters

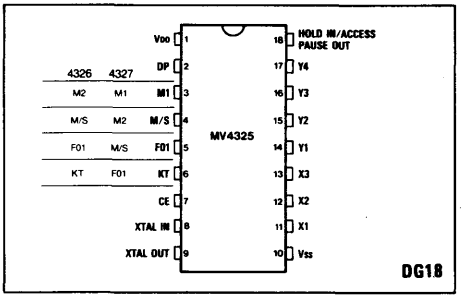

Fig.1 Pin connections (top view)

FEATURES

- Last Number Redial
- Multiple Access Pause Programming
- Any Valid Keypad Input or HOLD IN Causes Exit from Access Pause
- Oscillator Start Up Controlled from Keypad Input
- Oscillator Power Down whilst not Dialling
- 300 Hz Key Tone indicates Valid Key
- 2.0V to 7.0V Supply Voltage Operating Range
- Stores up to 20 Digits and Access Pauses
- Digit Memory Retained down to 1.0V at 1μA
- Selectable Mark/Space Ratio 66⅔ : 33⅓ or 60 : 40
- 10 Hz Dialling Speed (14.9 kHz Fast Test)

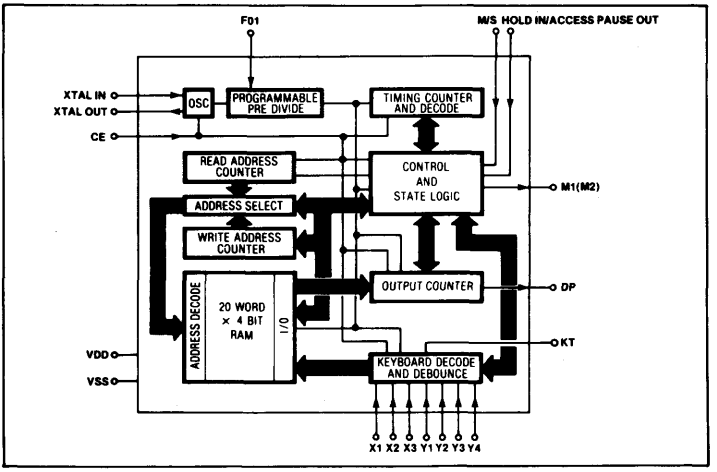

Fig.2 MV4325/MV4326 functional block diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN	MAX		MIN	MAX
$V_{DD}-V_{SS}$	-0.3V	10V			
Voltage on any pin	V_{SS}-0.3V	V_{DD} + 0.3V			
Current at any pin		10mA			
Operating Temperature	-40 °C	+85°C	Power Dissipation		1000mW
Storage Temperature	-65 °C	+ 150 °C			

* Derate 16mW/ °C above 75 °C. All leads soldered to PC board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, f_{CLK} = 3.579545MHz; V_{DD} = +3.0V
All voltages wrt V_{SS}

		CHARACTERISTIC		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.0		7.0	V		
2		Standby Supply Current		I_{DDS}			1.0	μA	CE = M/S = F01 = HOLD IN = V_{SS}, V_{DD} = 1.0V	
3		Operating Supply Current		I_{DD}		100	150	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-8.0	μA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, F01
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	8.0	μA	$V_{IN} = V_{DD}$	
8		Input Low Level Voltage		V_{IL}			0.9	V	All inputs	
9		Input High Level Voltage		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M_1, M_2, KT
13				I_{OL}	0.2	0.5		mA	V_{OUT} = 0.5V	
14			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	
15				I_{OH}	-0.2	-0.5		mA	V_{OUT} = 2.5V	
16	I/O	Input Low Level Voltage		V_{IL}			0.9	V		
17		Input High Level Voltage		V_{IH}	2.1			V		
18		Output Low Level Current		I_{OL}		15		μA	V_{OUT} = 0.5V	CE,
19		Output High Level Current		I_{OH}		-12		μA	V_{OUT} = 2.5V	HOLD IN/ACCESS
20		Input Force High Current (from V_{OL})		I_{FH}		55		μA	V_{IN} = 2.5V	PAUSE OUT
21		Input Force Low Current (from V_{OH})		I_{FL}		-70		μA	V_{IN} = 0.5V	

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = +25°C$; $f_{CLK} = 3.579545\,MHz$; $V_{DD} = +3.0V$

		CHARACTERISTIC	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	f_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio	M/S		2:1			M/S = O/C (V_{SS})
5					3:2			M/S = V_{DD}
6		System Clock Frequency (Internal)			300		Hz	F01 = V_{SS}
7		Impulsing Rate = I/T			10		Hz	F01 = V_{SS}
8		Fast Test Impulsing Rate			14.9		kHz	F01 = V_{DD}
9		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE ↑ '1'
10		Input Capacitance	C_{in}		5.0		pF	Any Input

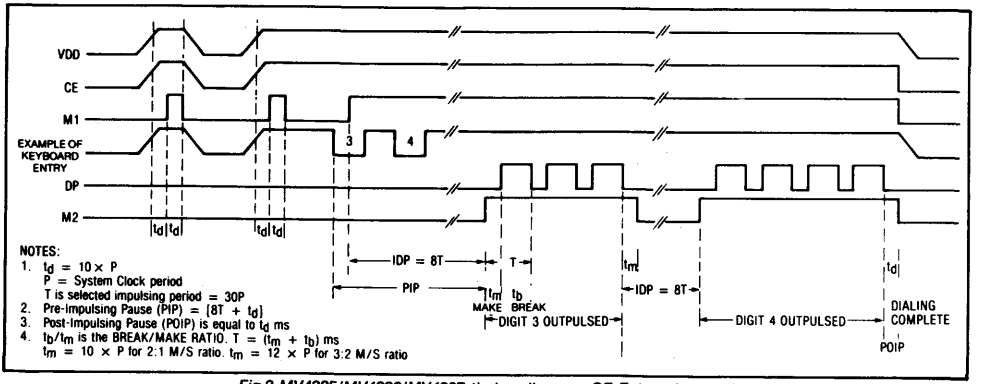

Fig.3 MV4325/MV4326/MV4327 timing diagram, CE External control

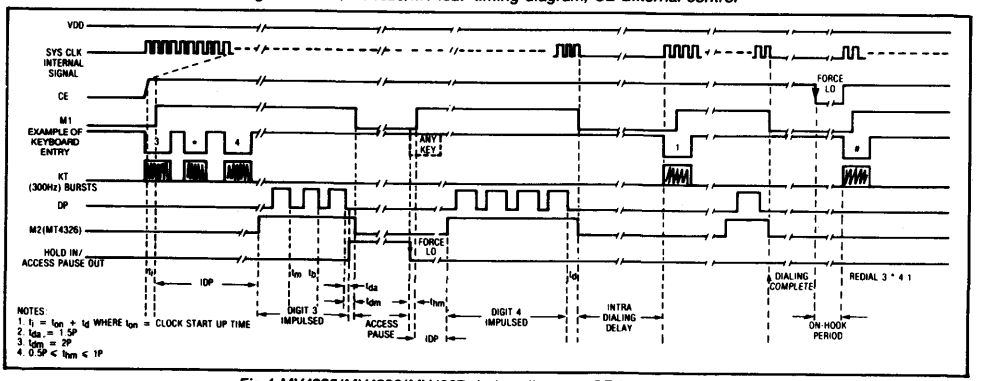

Fig.4 MV4325/MV4326/MV4327 timing diagram, CE Internal control

PIN FUNCTIONS

V_{DD}	Positive voltage supply				
DP	Dial Pulsing Output Buffer				
M1 (M2)	Mute Output Buffer				
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}. Note: O/C = Open Circuit			O/C	2:1
				V_{DD}	3:2
F01	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}. * Assumes f_{CLK} = 3.579545MHz.	F01	Nominal Impulsing Rate	Actual* Inpulsing Rate	System Clock frequency
		O/C	10Hz	10.13Hz	303.9Hz
		V_{DD}	14.9kHz	14,915Hz	447.4kHz
CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.				
XTAL IN	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.				
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.				
V_{SS}	System ground				
X_1,X_2,X_3	Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
Y_1,Y_2,Y_3,Y_4	Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
HOLD IN/	INPUT/OUTPUT	O/C	Normal Operation		
ACCESS	INPUT	V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete.		
PAUSE OUT	OUTPUT	V_{DD}	Logic "1" level output indicates access pause condition.		
KT	300Hz	Square wave bursts indicate valid keypad input.			

		KEYPAD INPUT CODE						
No. of O/P Pulses	Digit	Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0
ACCESS PAUSE		1	1	1	0	0	1	1

Table 1

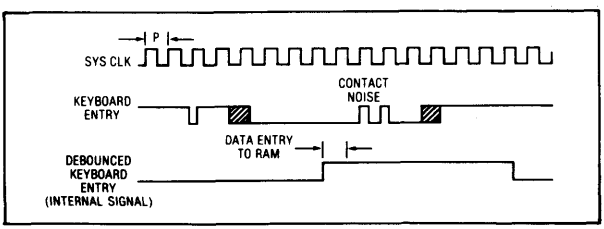

Fig.5 Keypad input debounce timing diagram

OPERATING NOTES

The MV4325 programmable keypad pulse dialer is optimized for use in key operated pulse dialling telephone sets and contains features which make it particularly suitable for applications where redial of last number dialled and repertory dial facilities are required.

Keypad information is accepted directly from a dual contact keypad having two single pole switches per key: one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the common column contacts connected X1 to X3. The other side of each switch is connected to a common VSS line. The keypad code is shown in Table 1.

The MV4325 will accept up to 20 digits and access pauses, e.g. 18 digits plus 2 access pauses or alternately 19 digits plus 1 access pause. Prior to a keypad input being accepted contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10ms is rejected and any input valid for greater than 17ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Fig.5.

The first key entered in any dialling sequence initiates the oscillator on the MV4325 by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in Fig.3 and Fig.4. Fig.3 shows use of the MV4325 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Fig.4 shows the timing diagram of the MV4325 including access pause and redial mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialling commences after recognition of the leading edge of the first valid key input. When an access pause is reached M1 (and M2 on the MV4326) goes low and Hold In/Access Pause Out goes high indicating the device is in an access pause. This output signal can be used to enable an external dial tone recognition circuit. Exit from the access pause is achieved by one of two methods. One method is by the next valid key operation. If a valid digit is entered, the digit will be entered in the next consecutive storage location in the digit memory. If the key # is activated, redialling of the number in memory will occur only if the device is in the redial mode. The alternative method to exit from an access pause is to pulse Hold In/Access Pause Out low, resetting the output latch associated with this input/output pin.

Fig.4 shows a pause in dialling between the completion of dialling digit 4 and keying digit 1. In this condition, the oscillator powers down to minimize power consumption and interfering signals, whilst CE remains high. On recognition of the next digit, the digit is entered in the next consecutive memory location and dialling resumes.

The end of a key entry sequence is indicated to the MV4325 by externally pulsing or clamping CE low. This causes the on-chip latch holding CE high to reset.

If the first key entered after a CE low period is #, redial of the last number dialled will occur. Access pause operation is as previously described. In the standby condition the MV4325 dissipates less than 1.0μW.

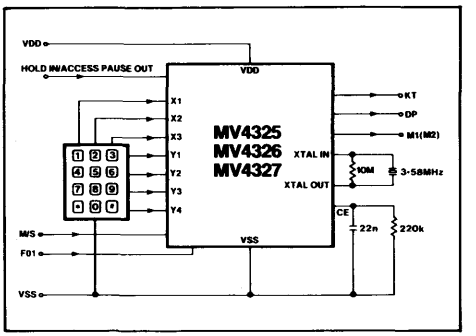

Fig.6 Application diagram

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MV4330 MV4332

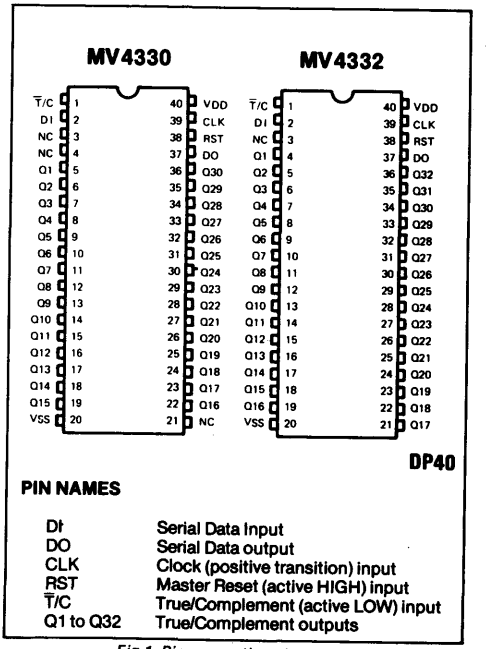
CMOS/LSI 30/32-BIT STATIC SHIFT REGISTERS WITH PARALLEL TRUE/COMPLEMENT OUTPUTS

The MV4330 and MV4332 are CMOS/LSI 30 and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alpha-numeric displays plus decimal points or two 16-segment alpha-numeric displays directly.

The devices are available in 40-pin plastic DIL (DP) package.

FEATURES

- Direct LCD Drive
- CMOS Low Power (1 μA)
- 3 to 18 Volt Operation
- On-Chip Wave-Shaping
- High Speed (Typ. 3 MHz) Shift Register



PIN NAMES

DI	Serial Data Input
DO	Serial Data output
CLK	Clock (positive transition) input
RST	Master Reset (active HIGH) input
T/C	True/Complement (active LOW) input
Q1 to Q32	True/Complement outputs

Fig.1 Pin connections (top view)

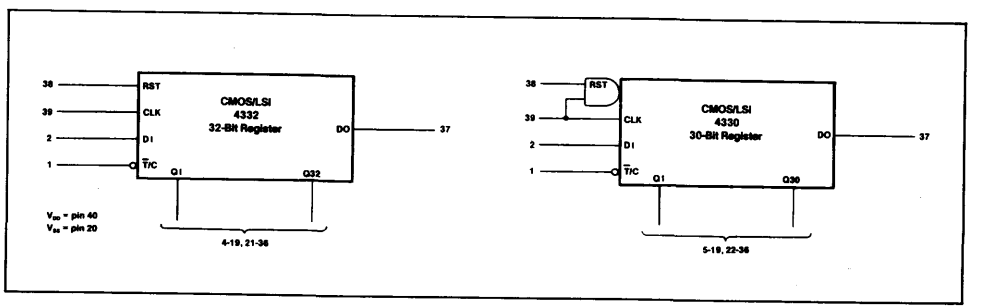


Fig.2 Block diagrams

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	VO Volts	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Quiescent Device Current		I_L			5	–	0.5	50	uA
					10	–	1	100	
Output Voltage	Low-Level	V_{OL}			5	–	0	0.01	V
					10	–	0	0.01	
	High-Level	V_{OH}			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		V_{NL}		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		V_{NH}		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	I_{DN}	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		I_{DP}	P-Channel	4.5	5	−0.35	−0.9	–	
				9.5	10	−0.8	−1.9	–	
	Q OUT	I_{DN}	N-Channel	0.5	10	50	250	–	uA
		I_{DP}	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $C_L = 50pF$
All input rise and fall times = 20ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Propagation Delay Time	tPHL tPLH		10	–	300	–	ns
Transition Time	tTHL	D OUT (CL=50pF)	10	–	70	130	ns
	tTLH	Q OUT (CL=15pF)	10	–	300	–	ns
Maximum Clock Frequency	fCL		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	tWL tWH		10	–	200	–	ns
Minimum Reset Pulse Width	tWH(R)		10	–	200	–	ns
Input Capacitance	CI	Any Input		–	5	–	pF

Note 1.Voltages with respect to V_{SS}
Note 2.Typical temperature coefficient for all values = 0.3%/°C

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	LIMIT	UNIT
DC Supply Voltage	VDD	-0.5 to 18	V
Input Voltage	VIN	-0.5 to VDD+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Ts	-65 to 125	°C

OPERATING NOTES

The MV4330 and MV4332 accept a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of these devices is that the clock input and the true/complement control (T/C) input have wave-shaping circuits (Fig.3) to ensure fast edges on-chip regardless of the shape of the incoming signals.

The MV4330 also has the reset (RST) input gated with the clock input for synchronous reset on the positive transition of the clock. The MV4332 has asynchronous reset (RST) inputs which are active HIGH.

The parallel outputs of the shift registers are available in either true or complementary form dependent on the state of the true/complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in each register. This action is independent of the clock input condition. A serial data (DO) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

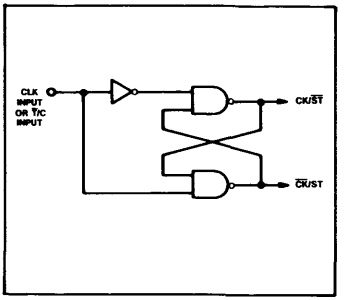


Fig.3 Wave shaping circuit

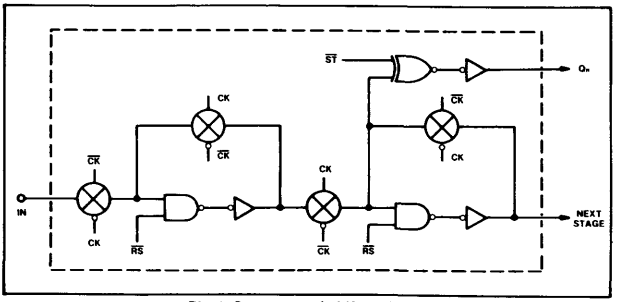


Fig.4 One stage of shift register

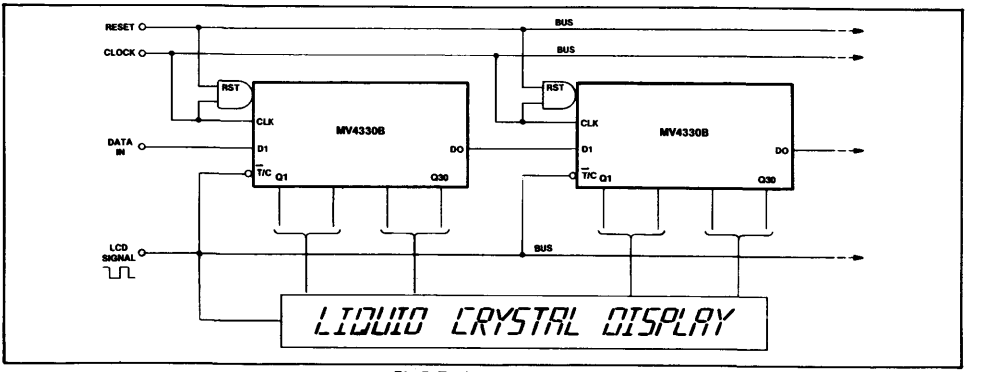


Fig.5 Typical application

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Semiconductors

ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV5087

DTMF GENERATOR

The MV5087 is fabricated using Plessey Semiconductors' ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with either a standard 2-of-8, or single contact (form A), keyboard. The keyboard entries determine the correct division of the reference frequency by the row and column counters.

D-to-A conversion, using R-2R ladder networks, results in a staircase approximation of a sinewave with low total distortion.

Frequency and amplitude stability over operating voltage and temperature range are maintained within industry DTMF specifications.

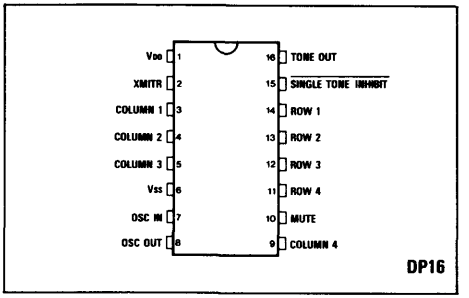

Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5087
- Low Standby Power
- Minimum External Parts Count
- 2.75V to 10V Operation
- 2-of-8 Keyboard or Calculator-Type Single Contact (Form A) Keyboard Input
- On-Chip Regulation of Output Tone
- Mute and Transmitter Drivers On-Chip
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point-of-Sale and Banking Terminals
- Process Control

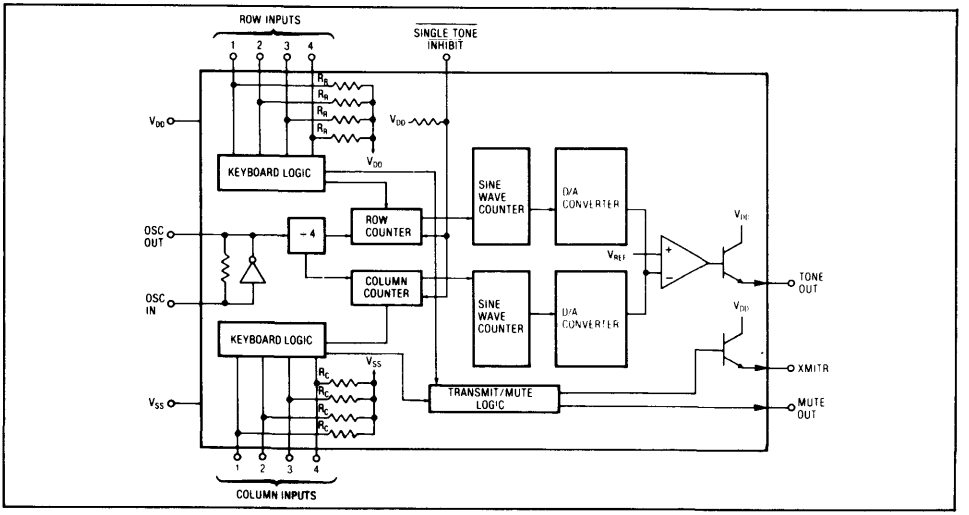

Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX		MIN.	MAX.
V_{DD}-V_{SS}	−0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} − 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	−40°C	+85°C			
Storage temperature	−65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	2.75		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	SINGLE TONE INHIBIT	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
		INPUT RESISTANCE	R_{IN}		60		KΩ		
	ROW 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.9V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.3V_{DD}	V		
	COLUMN 1-4	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}			V		
		INPUT LOW VOLTAGE	V_{IL}			0.1V_{DD}	V		
OUTPUTS	XMITR	SOURCE CURRENT	I_{OH}	-15	−25		mA	V_{DD} = 3V, V_{OH} = 2V	No Keyboard Entry
				-50	−100		mA	V_{DD} = 10V, V_{OH} = 8V	
		LEAKAGE CURRENT	I_{OZ}		0.1	10	uA	V_{DD} = 10V, V_{OH} = OV	Keyboard Entry
	MUTE	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3V, V_{OL} = 0.5V	No Keyboard Entry
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		SOURCE CURRENT	I_{OH}	-0.5			mA	V_{DD} = 3V, V_{OH} = 2.5V	Keyboard Entry
				-1.0			mA	V_{DD} = 10V, V_{OH} = 9.5V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	ROW TONE OUTPUT VOLTAGE	V_{OR}	320	400	500	mV_{RMS}	Single Tone R_L = 1KΩ
	COLUMN TONE OUTPUT VOLTAGE	V_{OC}	400	500	630	mV_{RMS}	
	EXTERNAL LOAD IMPEDANCE	R_L	700			Ω	V_{DD} = 3V
			330			Ω	V_{DD} = 10V
OUTPUT DISTORTION					−20	dB	Total out-of-band power relative to sum of row and column fundamental power
PRE EMPHASIS, High Band			1		3	dB	
Tone Output Rise Time		t_r		3	5	ms	

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	XMITR	Emitter output of a bipolar transistor whose collector is connected to V_{DD}. With no keyboard input this output remains at V_{DD} and a keyboard input changes the output to a high impedance state. The state of Single Tone Inhibit input has no effect on XMITR output.
3,4,5,9	Column 1-4	These inputs are held at V_{SS} by resistors Rc and sense a valid logic level (approx $1/2$ V_{DD}) when tied to a Row input.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC In, OSC Out	On-chip inverter completes the oscillator when a 3,579545 MHz crystal is connected to these pins. OSC In is the invertor input and OSC Out is the output.
10	Mute	This CMOS Output switches to V_{SS} with no keyboard input and to V_{DD} with a keyboard input. This output is unaffected by the state of Single Tone Inhibit.
11,12,13,14	Row 1-4	These inputs are held at V_{DD} by resistors R_R and sense a valid logic level (Approx $1/2$ V_{DD}) when tied to a column input.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-up resistor to V_{DD} and when left unconnected or tied to V_{DD}, single or dual tones may be generated. When V_{SS} is applied dual tones only are generated and no input combinations will cause generation of a single tone.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes, and regulates the output level of, the row and column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard, single contact (form A) keyboard and electronic input. Figures 3 and 4 show these input configurations, and Fig. 5 shows the internal structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed. Single tones are generated when more than one button is pushed in any row or column. No tones are generated when diagonally-positioned buttons are simultaneously pressed.

An electronic input to a single column generates that single column tone. Inputs to multiple columns generates no tone. An electronic input to a single row generates no tone and a single row tone may be generated only by activating 2 columns and the desired row.

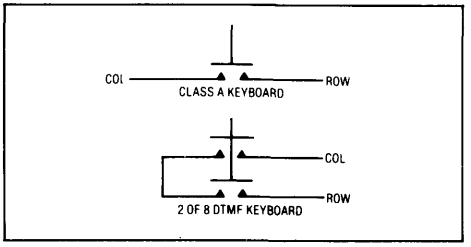

Fig.3 Keyboard configuration

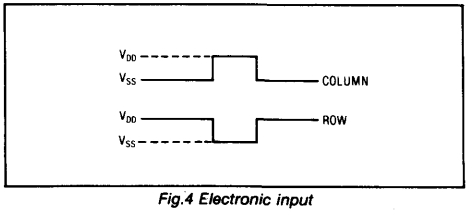

Fig.4 Electronic input

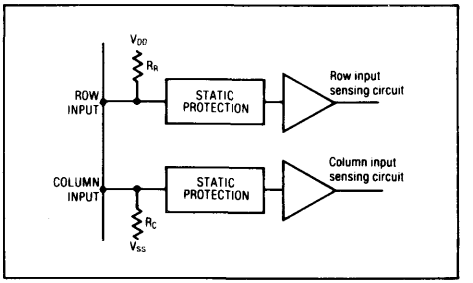

Fig.5 Row and column inputs

OUTPUT FREQUENCY

Table 1 shows the output frequency deviation from the standard DTMF frequencies when a 3.58MHz crystal is used as the reference.

The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6), resulting in a 'staircase' approximation to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
	f_7	1477	1471.9	-0.35	
	f_8	1633	1645.0	+0.73	

Table 1 Output frequency deviation

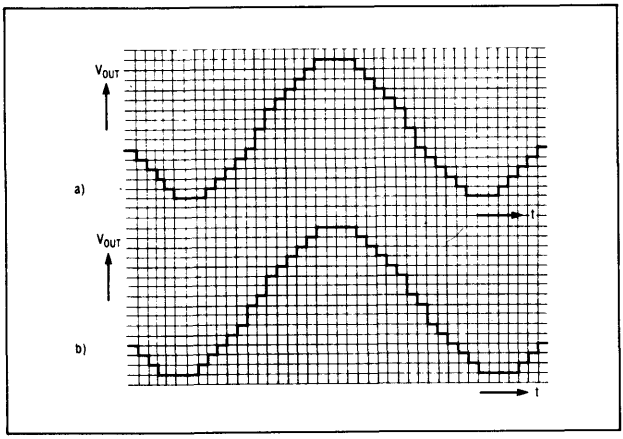

Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \cdots V_{nf}^2}}{V_{fundamental}}\right)\%$$

Where $V_{2f} - V_{nf}$ are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \cdots V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \cdots V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
$V_{2R} - V_{nR}$ are the Fourier component amplitudes of the row frequencies
$V_{2C} - V_{nC}$ are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

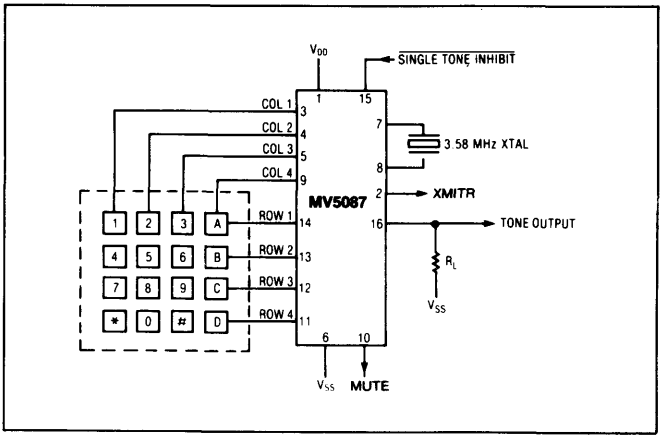

Fig.7 Connection diagram

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MV5089

DTMF GENERATOR

The MV5089 is fabricated using Plessey Semiconductors' ISO-CMOS high density technology and offers low power and wide voltage operation. An inexpensive 3.58MHz TV crystal completes the reference oscillator. From this frequency are derived 8 different sinusoidal frequencies which, when appropriately mixed, provide Dual-Tone Multi-Frequency (DTMF) tones.

Inputs are compatible with a standard 2-of-8 active-low keyboard and the keyboard entries determine the correct division of the reference frequency by the row and column counters. D-to-A conversion, using R-2R ladder networks, results in a 'staircase' approximation of a sinewave with low total distortion.

Frequency stability over operating voltage and temperature range are maintained within industry DTMF standards.

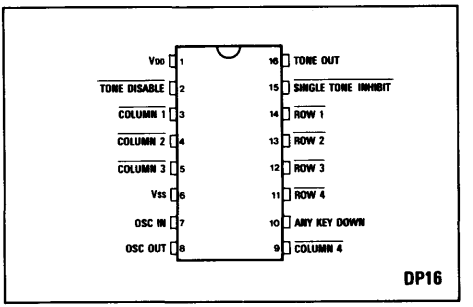

Fig.1 Pin connections - top view

FEATURES

- Pin-for-Pin Replacement for MK5089
- Low Standby Power
- Minimum External Parts Count
- 2.75V to 10V Operation
- 2-of-8 Keyboard Input
- High Accuracy Tones Provided by 3.58MHz Crystal Oscillator
- Pin-Selectable Inhibit of Single Tone Generation

APPLICATIONS

DTMF Signalling for

- Telephone Sets
- Mobile Radio
- Remote Control
- Point of Sale and Banking Terminals
- Process Control

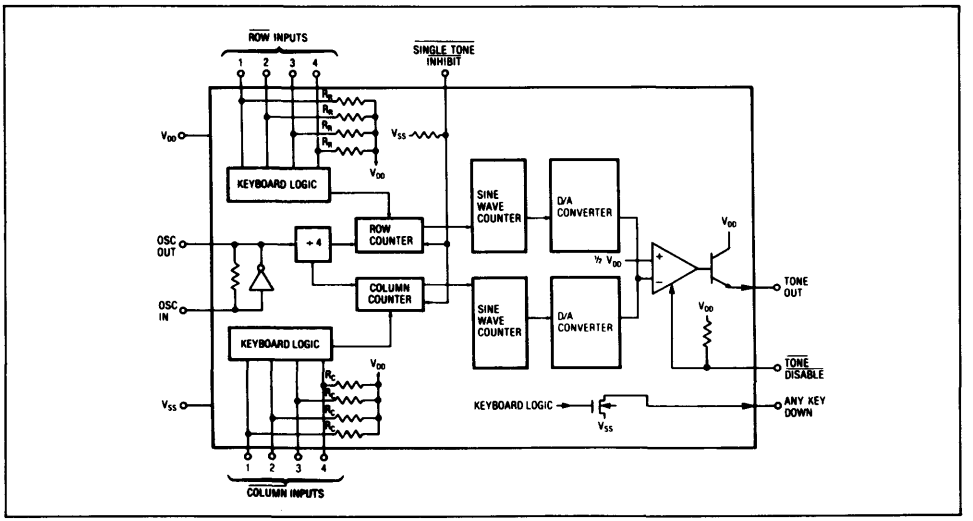

Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS

	MIN.	MAX		MIN.	MAX.
V_{DD}-V_{SS}	−0.3V	10.5V	Power dissipation		850 mW
Voltage on any pin	V_{SS} − 0.3V	V_{DD} + 0.3V	Derate 16 mW/°C above 75°C		
Current on any pin		10 mA	(All leads soldered to PCB)		
Operating temperature	−40°C	+85°C			
Storage temperature	−65°C	+150°C			

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

	CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS		
SUPPLY	Operating Supply Voltage		V_{DD}	2.75		10	V	Ref. to V_{SS}	
	Standby Supply Current		I_{DDS}		0.2	100	uA	V_{DD} = 3V	No Key Depressed
					0.5	200	uA	V_{DD} = 10V	All outputs Unloaded
	Operating Supply Current		I_{DD}		1.0	2.0	mA	V_{DD} = 3V	One Key Depressed
					5.0	10.0	mA	V_{DD} = 10V	All outputs Unloaded
INPUTS	$\overline{\text{SINGLE TONE}}$ $\overline{\text{INHIBIT}}$. $\overline{\text{TONE DISABLE}}$	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
		INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
		INPUT RESISTANCE	R_{IN}		60		KΩ		
	$\overline{\text{ROW 1-4}}$	INPUT HIGH VOLTAGE	V_{IH}	0.7V_{DD}		V_{DD}	V		
	$\overline{\text{COLUMN 1-4}}$	INPUT LOW VOLTAGE	V_{IL}	0		0.3V_{DD}	V		
OUTPUTS	ANY KEY DOWN	SINK CURRENT	I_{OL}	0.5			mA	V_{DD} = 3V, V_{OL} = 0.5V	
				1.0			mA	V_{DD} = 10V, V_{OL} = 0.5V	
		LEAKAGE CURRENT	I_{OZ}		1		uA	V_{DD} = 3V	

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{DD} = 3V to 10V

CHARACTERISTICS		SYMBOL	MIN	TYP	MAX	UNITS	
TONE OUT	OUTPUT LEVEL, ROW	V_{OUT}	-10	−8	-7	dBm	V_{DD} = 3V. Single Tone. R_L = 100KΩ
PRE EMPHASIS, High Band			2.4	2	3.0	dB	
OUTPUT DISTORTION (Dual Tone)					−20	dB	Total out-of-band power relative to sum of row and column fundamental power
Tone Output Rise Time		t_r		3	5	ms	Time for waveform to reach 90% of magnitude of either frequency from initial key stroke

PIN FUNCTIONS

PIN	NAME	DESCRIPTION
1	V_{DD}	Positive Power Supply
2	$\overline{\text{TONE DISABLE}}$	This input has an internal pull-up resistor to V_{DD}. When connected to V_{SS} no tones are generated by any key depression allowing the keyboard to be used for purposes other than DTMF signalling.
3,4,5,9	$\overline{\text{COLUMN 1-4}}$	These CMOS inputs are held at V_{DD} by an internal pull-up resistor and are activated by the application of V_{SS}.
6	V_{SS}	Negative Power Supply (OV)
7,8	OSC IN, OSC OUT	On-chip inverter completes the oscillator when a 3,58 MHz Crystal is connected to these pins. OSC IN is the inverter input and OSC OUT is the output.
10	Any Key Down	This is an NMOS transistor output which switches to V_{SS} when any key is depressed. Otherwise this output is high impedance. Switching is independent of $\overline{\text{Tone Disable}}$ and $\overline{\text{Single Tone Inhibit}}$.
11,12,13,14	$\overline{\text{Row 1-4}}$	As $\overline{\text{Column 1-4}}$ inputs.
15	$\overline{\text{Single Tone Inhibit}}$	This input has a pull-down resistor to V_{SS}. When left unconnected or tied to V_{SS}, dual tones may be generated, but keyboard input combinations resulting in single tone generation are inhibited. When V_{DD} is applied single or dual tones may be generated.
16	Tone Out	Emitter output of a bipolar NPN transistor whose collector is tied to V_{DD}. Input to this transistor is from an op-amp which mixes the Row and Column tones.

ROW AND COLUMN INPUTS

These inputs are compatible with the standard 2-of-8 keyboard or with an electronic input. Figures 3 and 4 show these input configurations and Fig.5 shows the internal chip structure of these inputs.

When operating with a keyboard, dual tones are generated when any single button is pushed.

With Single Tone Inhibit at V_{DD}, connection of V_{SS} to a single column causes the generation of that Column tone. Connection of V_{SS} to more than one Column will result in no Column tones being generated. Connection of V_{SS} to Rows only generates no tone - a Column must be connected to V_{SS}.

A single Row tone only may be generated by connecting 2 columns, and the desired row, to V_{SS}.

OUTPUT TONE LEVEL

The output tone level of the MV5089 is proportional to the applied DC supply voltage.

A regulated supply will normally be used which may be designed to provide stability over the temperature range.

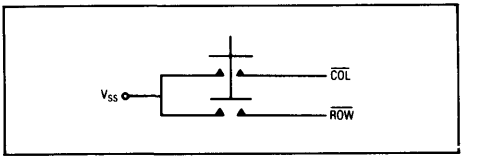

Fig.3 2 of 8 DTMF keyboard

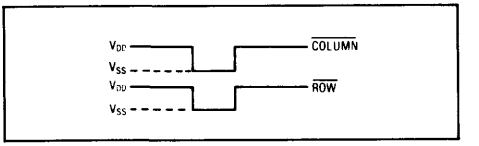

Fig.4 Electronic input

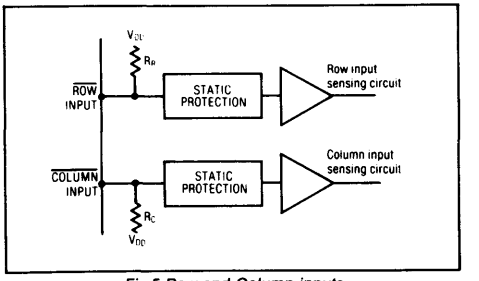

Fig.5 Row and Column inputs

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The row and column output waveforms are digitally synthesised using R-2R D-to-A converters (see Fig.6) resulting in staircase approximations to a sinewave. An op-amp mixes these tones to produce a dual-tone waveform. Single tone distortion is typically better than 7% and all distortion components of the mixed dual-tone should be -30dB relative to the strongest fundamental (column tone).

		Standard DTMF (Hz)	Tone Output Frequency Using 3.579545 MHz Crystal	% Deviation From Standard	
Row	f_1	697	701.3	+0.62	Low Group
	f_2	770	771.4	+0.19	
	f_3	852	857.2	+0.61	
	f_4	941	935.1	-0.63	
Column	f_5	1209	1215.9	+0.57	High Group
	f_6	1336	1331.7	-0.32	
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Table 1 Output frequency deviation

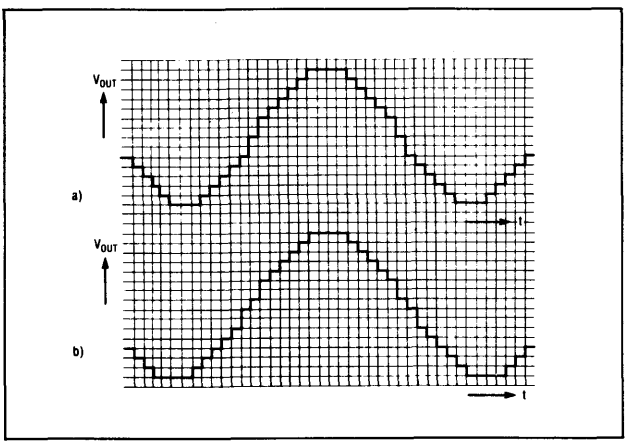

Fig.6 Typical sinewave output (a) Row tones (b) Column tones

DISTORTION MEASUREMENTS

THD for the single tone is defined by:

$$100\left(\frac{\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \text{----} V_{nf}^2}}{V_{\text{fundamental}}}\right)\%$$

Where V_{2f} -- V_{nf} are the Fourier components of the waveform.

THD for the dual tone is defined by:

$$100\left(\frac{\sqrt{V_{2R}^2 + V_{3R}^2 \text{--} V_{nR}^2 + V_{2C}^2 + V_{3C}^2 \text{---} V_{nc}^2 + V_{IMD}^2}}{\sqrt{V_{ROW}^2 + V_{COL}^2}}\right)$$

where V_{ROW} is the row fundamental amplitude
V_{COL} is the column fundamental amplitude
V_{2R} -- V_{nR} are the Fourier component amplitudes of the row frequencies
V_{2C} -- V_{nC} are the Fourier component amplitudes of the column frequencies
V_{IMD} is the sum of all intermodulation components.

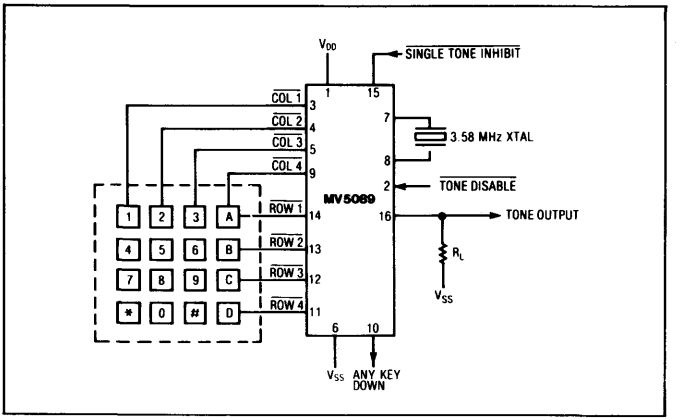

Fig.7 connection diagram

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MV74SC137, MV74SC138, MV74SC139 MV74SC237, MV74SC238, MV74SC239

OCTAL DECODERS/DEMULTIPLEXERS

This family of ISO-CMOS MSI circuits is designed for use in high speed memory and peripheral address decoding systems. MV74SC138 and MV74SC238 decode 3 binary inputs (A_0, A_1, A_2) to select one of eight mutually exclusive outputs ($O_0 - O_7$). Three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3), reduce the need for external gates in an expanded system. MV74SC137 and MV74SC237 feature additional latches on A_0, A_1 and A_2 for use in glitch free applications. When Latch Enable (LE) is LOW the device acts as MV74SC138. When LE is HIGH the address present at A_0 to A_2 is stored. A 1 of 32 decoder requires only four of these devices and one inverter. MV74SC139 and MV74SC239 feature two individual, two line (A_0, A_1) to four line ($O_0 - O_3$) decoders. Each decoder has an active LOW Enable ($\overline{E}$) which can also be used as a data input in a full four-minterm of two variables decode, as shown in Fig.8.

The devices are available in the 16-pin ceramic DIL (DG) package.

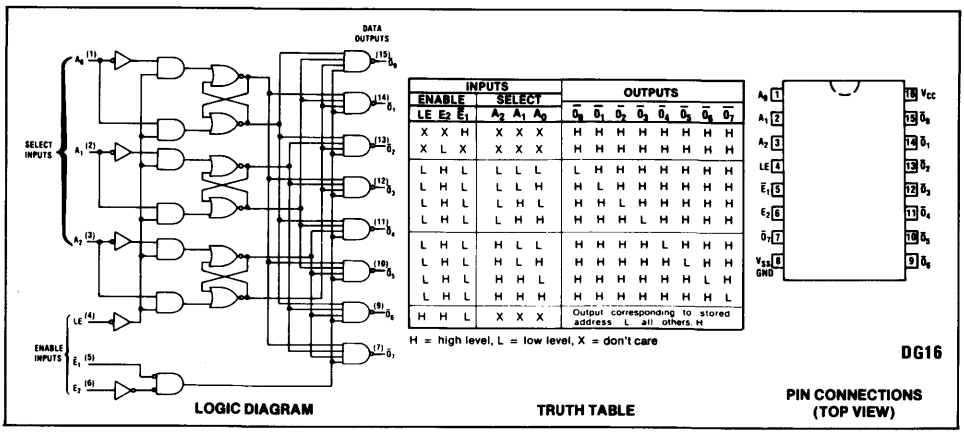
FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- High Current, Sink/Source Capability

DEVICE SELECTION

Product	Format	Output
MV74SC137	1 of 8, latched address	inverted
MV74SC138	1 of 8	inverted
MV74SC139	Dual 1 of 4	inverted
MV74SC237	1 of 8, latched address	non-inverted
MV74SC238	1 of 8	non-inverted
MV74SC239	Dual 1 of 4	non-inverted

FUNCTIONAL BLOCK DIAGRAMS AND LOGIC



LOGIC DIAGRAM

INPUTS						OUTPUTS							
ENABLE			SELECT										
LE	$\overline{E}_2$	$\overline{E}_1$	A_2	A_1	A_0	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L all others H							

H = high level, L = low level, X = don't care

TRUTH TABLE

DG16

PIN CONNECTIONS (TOP VIEW)

Fig.1 MV74SC137

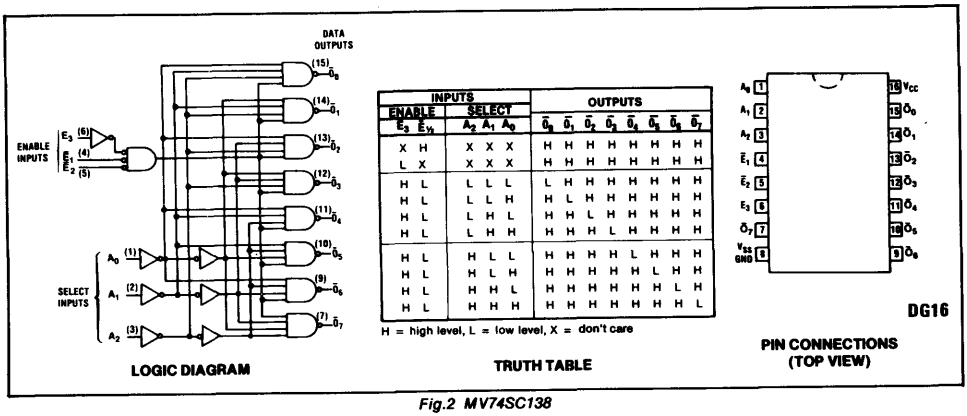


Fig.2 MV74SC138

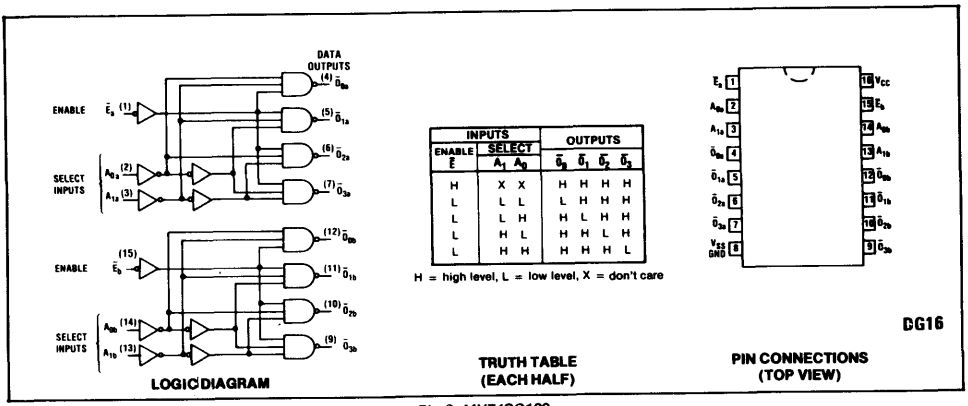


Fig.3 MV74SC139

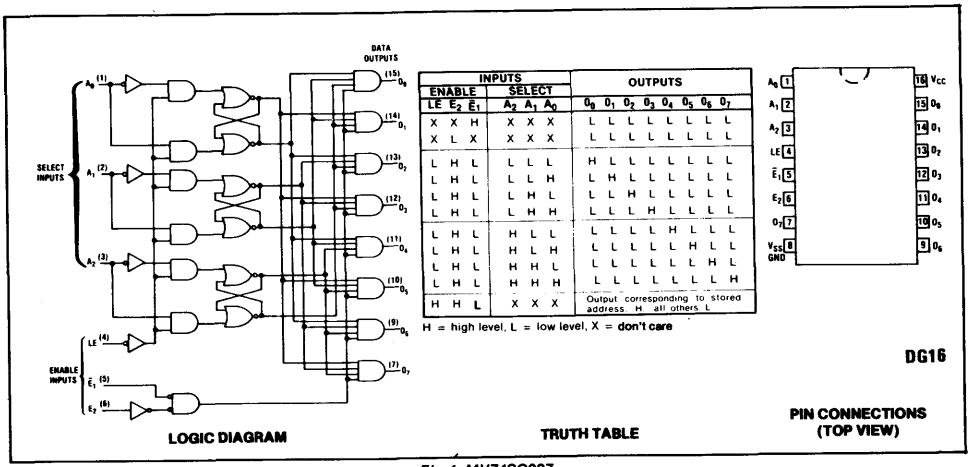
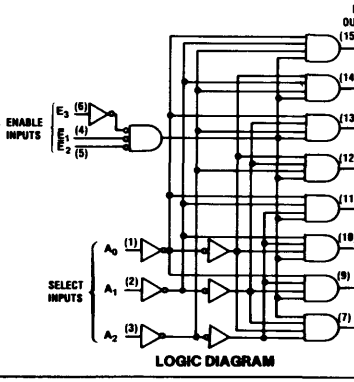


Fig.4 MV74SC237



INPUTS				OUTPUTS
ENABLE		SELECT		
$\bar{E}_3$	$\bar{E}_{1/2}$	A_2	A_1 A_0	$\bar{O}_0$ $\bar{O}_1$ $\bar{O}_2$ $\bar{O}_3$ $\bar{O}_4$ $\bar{O}_5$ $\bar{O}_6$ $\bar{O}_7$
X	H	X	X X	L L L L L L L L
L	X	X	X X	L L L L L L L L
H	L	L	L L	H L L L L L L L
H	L	L	L H	L H L L L L L L
H	L	L	H L	L L H L L L L L
H	L	L	H H	L L L H L L L L
H	L	H	L L	L L L L H L L L
H	L	H	L H	L L L L L H L L
H	L	H	H L	L L L L L L H L
H	L	H	H H	L L L L L L L H

H = high level, L = low level, X = don't care

TRUTH TABLE

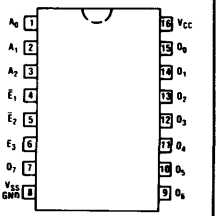
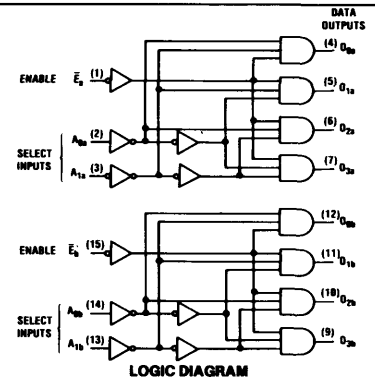


Fig.5 MV74SC238



INPUTS		OUTPUTS
ENABLE	SELECT	
$\bar{E}$	A_1 A_0	$\bar{O}_0$ $\bar{O}_1$ $\bar{O}_2$ $\bar{O}_3$
H	X X	L L L L
L	L L	H L L L
L	L H	L H L L
L	H L	L L H L
L	H H	L L L H

H = high level, L = low level, X = don't care

TRUTH TABLE (EACH HALF)

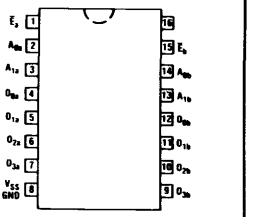


Fig.6 MV74SC239

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis ($V_{T+} - V_{T-}$)			0.3		V	
High level output voltage	V_{OH}	2.4 4.00			V V	V_{CC} = 4.75V, I_{OH} = −14mA I_{OH} = −3mA
Low level output voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 10mA
Input current at maximum input voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High level input current	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			−10	µA	V_{CC} = 5.25V, V_I = 0.4V
Short circuit output current (2)	I_{OS}		−40		mA	V_{CC} = 5.25V
Supply current	I_{CC}			0.1	mA	V_{CC} = 5.25V, outputs open

1. All TYP. values at T_{amb} = 25°C V_{CC} = 5V
2. Max. dissipation or 1ms duration should not be exceeded.

SWITCHING CHARACTERISTICS

Test conditions (unless otherwise stated):
$V_{CC} = 5V$, $T_{amb} = +25°C$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS C_L = 15pF, R_L = 2K
Propagation delay time Address to output	t_{PLH}		30	50	nS	
Propagation delay time Address to output	t_{PHL}		31	52	nS	
Propagation delay time E_2 or E_1 to output	t_{PLH}		33	45	nS	MV74SC137 and MV74SC237
Propagation delay time E_2 or E_1 to output	t_{PHL}		34	52	nS	
Propagation delay time E to output	t_{PLH}		33	45	nS	MV74SC138 and MV74SC238
Propagation delay time E to output	t_{PHL}		34	52	nS	
Propagation delay time E to output	t_{PLH}		25	45	nS	MV74SC139 and MV74SC239
Propagation delay time E to output	t_{PHL}		30	53	nS	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}	3.0	5	7.0	V
High level output current	I_{OH}		−24		mA
Low level output current	I_{OL}		24		mA
Operating free-air temperature	T_A	0		70	°C

3. Voltages are with respect to V_{SS}/GND

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	−0.5V to 7.0V
Input voltage	V_I	−0.3V to V_{CC} + 0.3V
Output current, each output	I_O	±75mA
Operating temperature	T_A	−40°C to +85°C
Storage temperature	T_S	−65°C to 150°C
Package power dissipation	P	450mW

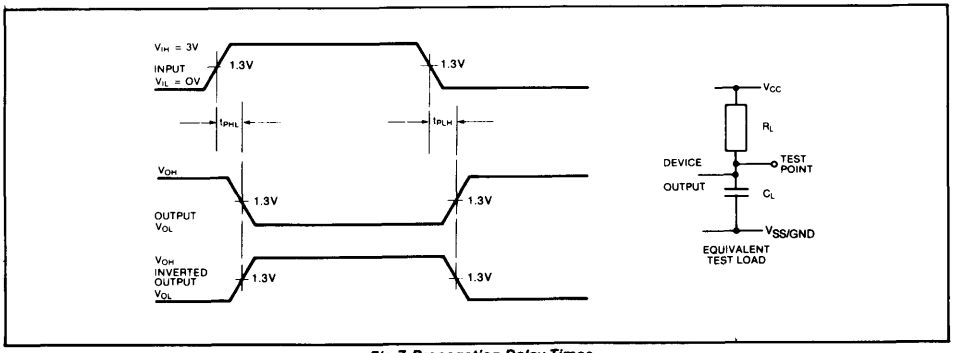


Fig.7 Propagation Delay Times

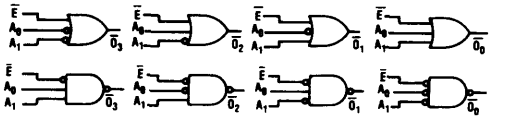


Fig.8 Logic Reduction Application: 4 minterms of 2 variables by MV74SC139

PIN FUNCTIONS

PIN	DESCRIPTION
A_0, A_1, A_2 or A_{0a}, A_{0b} A_{1a}, A_{1b}	Select (Address) Inputs, to be decoded
$\overline{E}_1$, $\overline{E}_2$, E_3 or $\overline{E}_a$, $\overline{E}_b$ or $\overline{E}_1$, E_2	Chip Enable Inputs
LE	Latch Enable Input
O_0 - O_7 or $\overline{O}_0$ - $\overline{O}_7$	Decoded Outputs Inverted Decoded Outputs
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

PLESSEY Semiconductors

ADVANCE INFORMATION CMOS

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MV74SC240, MV74SC241, MV74SC244 MV74SC540, MV74SC541

THREE-STATE OCTAL BUFFERS/LINE DRIVERS

This family of ISO-CMOS Octal Buffers and Line Drivers is designed to improve PC board density and performance in three-state memory address drivers, clock drivers and bus oriented receivers and transmitters. A comprehensive range of devices covers a selection of differing input/output pin layouts, inverting and non-inverting buffers and a choice of similar or complementary output controls ($\overline{E}_A$, $\overline{E}_B$).

The devices are available in the 20-pin DIL (DG) package.

FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- Bus Oriented 3-state outputs
- High Current Sink/Source Capability

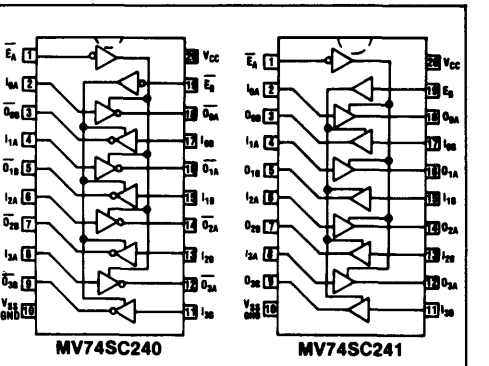

Fig.1 Pin connections (top view)

TRUTH TABLES

INPUTS		OUTPUT	
$\overline{E}$	$I_{0\text{-}3}$	MV74SC240 $O_{0\text{-}3}$	MV74SC244 $O_{0\text{-}3}$
L	L	H	L
L	H	L	H
H	X	Z	Z

A or B Buffers

MV74SC241					
A BUFFERS			B BUFFERS		
INPUTS		OUTPUT	INPUTS		OUTPUT
$\overline{E}_A$	$I_{0\text{-}3}$	$O_{0\text{-}3}$	$\overline{E}_B$	$I_{0\text{-}3}$	$O_{0\text{-}3}$
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

INPUTS			OUTPUT	
$\overline{E}_1$	$\overline{E}_2$	$I_{0\text{-}7}$	MV74SC540 $O_{0\text{-}7}$	MV74SC541 $O_{0\text{-}7}$
L	L	L	H	L
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z

L Logic Low
H Logic High
X Don't Care
Z High Impedance

DEVICE SELECTION

PRODUCT	3-STATE CONTROL	DATA OUTPUTS
MV74SC240	$\overline{E}_A$, $\overline{E}_B$	inverting
MV74SC241	$\overline{E}_A$, E_B	non-inverting
MV74SC244	$\overline{E}_A$, $\overline{E}_B$	non-inverting
MV74SC540	$\overline{E}_1$ AND $\overline{E}_2$	inverting
MV74SC541	$\overline{E}_1$ AND $\overline{E}_2$	non-inverting

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	−0.5V to 7.0V
Input voltage	V_I	−0.3V to Vcc + 0.3V
Output current, per output	I_O	±75mA
Operating temperature	T_A	−40°C to +85°C
Storage temperature	T_S	−65°C to 150°C
Package Power dissipation	P	450mW

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage	V_{CC}	3	5	7	V
High level output current	I_{OH}		−24		mA
Low level output current	I_{OL}		24		mA
Operating free-air temperature	T_{amb}	0		70	°C

1. Voltage values are with respect to V_{SS}/GND.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	Vcc = 4.75V
Hysteresis ($V_{T+} - V_{T-}$)	V_O		0.3		V	
High level output voltage	V_{OH}	2.4 4.0			V V	V_{CC} = 4.75V, I_{OH} = −14mA I_{OH} = −3mA
Low level output voltage	V_{OL}			0.4	V	V_{CC} = 4.75V, I_{OL} = 16mA
Off-state output current, high-level voltage applied	I_{OZH}			20	µA	V_{CC} = 5.25V, V_O = 2.7V
Off-state output current, low-level voltage applied	I_{OZL}			−20	µA	V_{CC} = 5.25V, V_O = 0.4V
Input current at maximum input voltage	I_I			15	µA	V_{CC} = 5.25V, V_I = 5.55V
High level input current	I_{IH}			10	µA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			−10	µA	V_{CC} = 5.25V, V_I = 0.4V
Short circuit output current	I_{OS}		−40		mA	NOTE 2 V_{CC} = 5.25V
Supply current	I_{CC}			0.1	mA	V_{CC} = 5.25V, outputs disabled

2. Max. dissipation or 1mS duration should not be exceeded.
3. All Typical values at T_A = 25°C V_{CC} = 5V

SWITCHING CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 5V, T_{amb} = +25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Propagation delay time, low-to-high-level output	t_{PLH}		26	45	nS	C_L = 45pF, R_L = 667
Propagation delay time, high-to-low-level output	t_{PHL}		27	45	nS	
Output enable time to low level	t_{PZL}		39	58	nS	C_L = 5pF, R_L = 667
Output enable time to high level	t_{PZH}		28	45	nS	
Output disable time from low level	t_{PLZ}		30	45	nS	
Output disable time from high level	t_{PHZ}		33	45	nS	

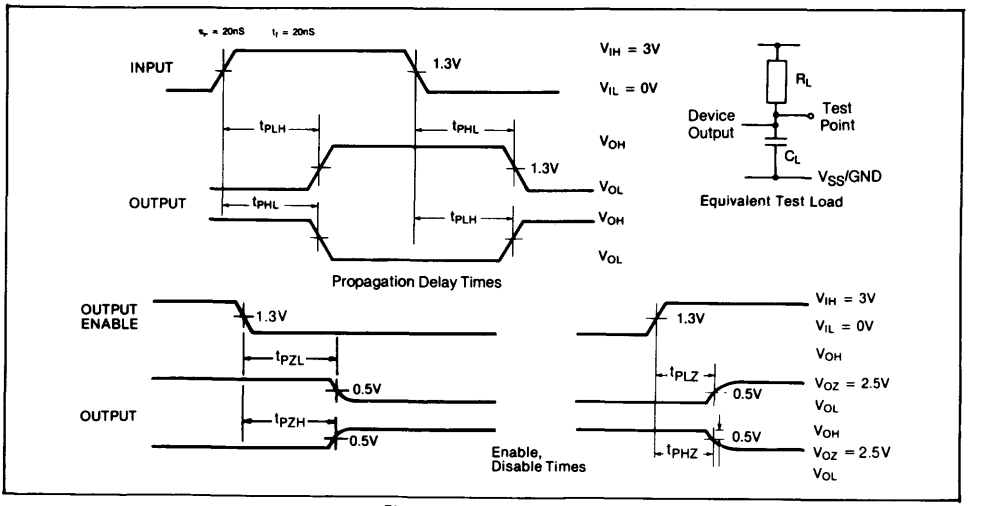

Fig.2 Voltage waveforms

PIN FUNCTIONS

PIN	DESCRIPTION
$\overline{E}_A$, $\overline{E}_B$ $\overline{E}_1$, $\overline{E}_2$ $\overline{E}_A$, E_B	Data Output Enable
I_{0A} - I_{3A} I_{0B} - I_{3B} or I_{0-7}	Data Inputs
O_{0A} - O_{3A} O_{0B} - O_{3B} or O_0 - O_7	Data Outputs
$\overline{O}_{0A}$ - $\overline{O}_{3A}$ $\overline{O}_{0B}$ - $\overline{O}_{3B}$ or $\overline{O}_0$ - $\overline{O}_7$	Inverted Data Outputs
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

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MV74SC245 MV74SC545

OCTAL BUS TRANSCEIVERS WITH 3-STATE BUFFERED OUTPUTS

These octal bus transceiver circuits are designed for high-speed asynchronous two-way communication between data buses. The control function inputs minimize external timing requirements.

The devices provide data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control input (DIR) pin. The enable input ($\overline{E}$) pin can be used to disable the device outputs so that the buses are effectively isolated from each other. The MV74SC545 differs from the MV74SC245 by use of inverting buffers.

The devices are available in 20-pin DIL(DG)package.

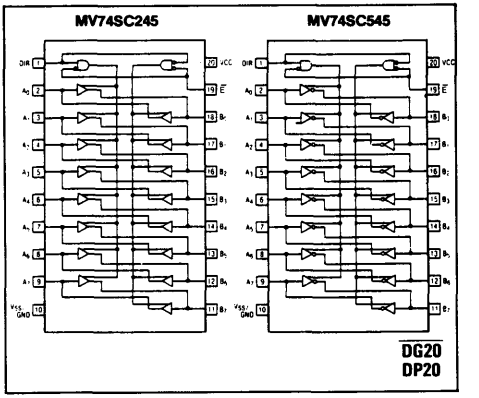

Fig.1 Pin connections and logic diagrams (top view)

FEATURES

- Pin Compatible with 74LS245 Types
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Bus Oriented 3-state Outputs
- Improved Noise Margins, with Input Hysteresis
- High Performance Input/Output Clamping
- Fully TTL compatible, Inputs and Outputs

PIN FUNCTION

Pin	Description
$A_0 \cdot A_7$	Bus A, Data Inputs/Outputs
$B_0 \cdot B_7$	Bus B, Data Inputs/Outputs
DIR	Direction Control Input
$\overline{E}$	Enable Input, Active LOW
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

FUNCTION TABLE

Enable $\overline{E}$	Direction Control DIR	Operation
L	L	B → A
L	H	A → B
H	X	Isolation

H = High Level, L = Low Level, X = Don't Care

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
High Level Input Voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low Level Input Voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis ($V_{T+} - V_{T-}$)			0.3		V	
High Level Output Voltage	V_{OH}	2.4 4.0			V V	V_{CC} = 4.75V I_{OH} = −14mA I_{OH} = −3mA
Low Level Output Voltage	V_{OL}			0.4	V	V_{CC} = 4.75V I_{OL} = 7mA
Offstate Output Current, High Level Voltage Applied	I_{OZH}			20	µA	V_{CC} = 5.25V V_O = 2.7V
Offstate Output Current, Low Level Voltage Applied	I_{OZL}			−20	µA	V_{CC} = 5.25V V_O = 0.4V
Input Current at Maximum Input Voltage	I_I			15	µA	V_{CC} = 5.25V V_I = 5.55V
High Level Input Current (Note 1)	I_{IH}			10	µA	V_{CC} = 5.25V V_{IH} = 2.7V
Low Level Input Current (1)	I_{IL}			−10	µA	V_{CC} = 5.25V V_{IL} = 0.4V
Short Circuit Output Current	I_{OS}		−40		mA	V_{CC} = MAX (Note 2)
Supply Current	I_{CC}			0.1	mA	V_{CC} = 5.25V Outputs disabled

Note 1. Inputs DIR and $\overline{E}$
Note 2. Max. dissipation or 1 ms should not be exceeded
Note 3. All Typ. values at T_A = 25°C, V_{CC} = 5V

SWITCHING CHARACTERISTICS

Test Conditions (unless otherwise stated):
V_{CC} = 5V T_{amb} = 25°C

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Propagation Delay Time Low to High Output	t_{PLH}		22		nS	C_L = 45pF R_L = 667Ω
Propagation Delay Time High to Low Input	t_{PHL}		25		nS	
Output Enable Time to Low Level	t_{PZL}		41		nS	
Output Enable Time to High Level	t_{PZH}		40		nS	
Output Disable Time from Low Level	t_{PLZ}		32		nS	C_L = 5pF R_L = 667Ω
Output Disable Time from High Level	t_{PHZ}		40		nS	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter	Symbol	Value
Supply Voltage	V_{CC}	−0.5V to 7.0V
Input Voltage	V_I	−0.3V to V_{CC} + 0.3V
Output Current	I_O	±75mA
Storage Temperature	T_S	−65°C to 150°C
Operating Temperature	T_{amb}	−40°C to 85°C
Power Dissipation	P	450mW

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3	5	7	V
High Level, Output Current	I_{OH}		−24		mA
Low Level, Output Current	I_{OL}		24		mA
Operating Temperature	T_{amb}	0		70	°C

Note: 4. Voltages are with respect to V_{SS}/GND

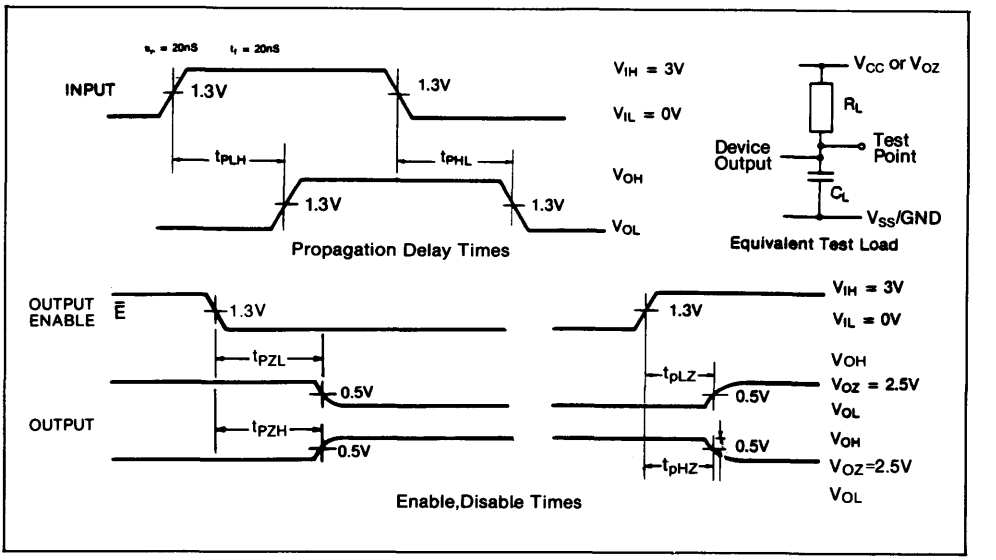

Fig.2 Voltage waveforms

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MV74SC373, MV74SC374, MV74SC533 MV74SC534, MV74SC563, MV74SC564 MV74SC573, MV74SC574

3-STATE OCTAL D-TYPE TRANSPARENT LATCHES AND EDGE TRIGGERED FLIP-FLOPS

This family of 8 bit latches features 3-state operation and is designed for use in high speed, bus oriented systems. The '373 appears transparent to data (outputs change asynchronously) when Latch Enable, $\overline{LE}$, is HIGH. When $\overline{LE}$ is LOW, data meeting the set up times becomes latched. The '374 latches hold their individual data when meeting set up times with the clock, CK, LOW-to-HIGH transition. With both devices $\overline{OE}$ does not affect the state of the latches, but when $\overline{OE}$ is HIGH the outputs become high impedance. Data may thus be latched even when the device is deselected. The family offers a choice of inverted or non-inverted outputs.

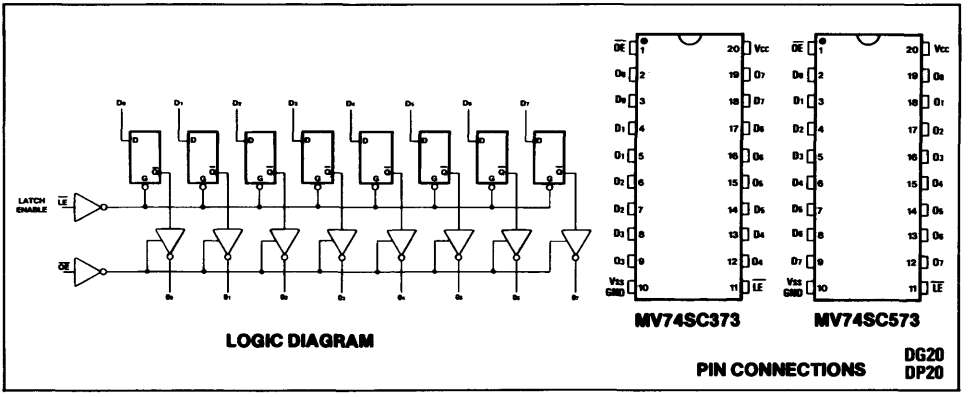
The devices are available in 20-lead ceramic DIL (DG) package.

FEATURES

- Equivalent to 74LS Series
- Low Power ISO-CMOS Technology
- Short Propagation Delay
- Improved Noise Margins, with Input Hysteresis
- Bus Oriented 3-State Outputs
- High Current, Sink/Source Capability

DEVICE SELECTION

Product	Format	Output
MV74SC373	transparent latch	non-inverted
MV74SC374	D type flip-flop	non-inverted
MV74SC533	transparent latch	inverted
MV74SC534	D type flip-flop	inverted
MV74SC563	transparent latch	inverted
MV74SC564	D type flip-flop	inverted
MV74SC573	transparent latch	non-inverted
MV74SC574	D type flip-flop	non-inverted



LOGIC DIAGRAM

PIN CONNECTIONS DG20 DP20

Fig.1 MV74SC373 and MV74SC573

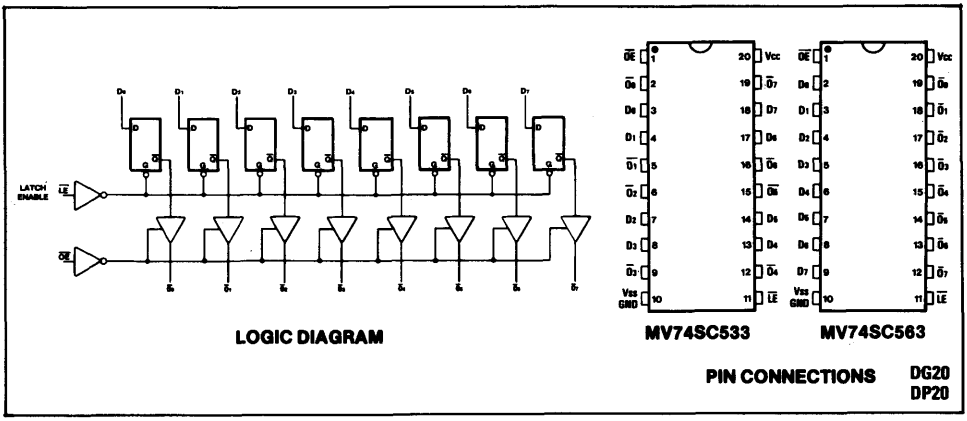


Fig.2 MV74SC533 and MV74SC563

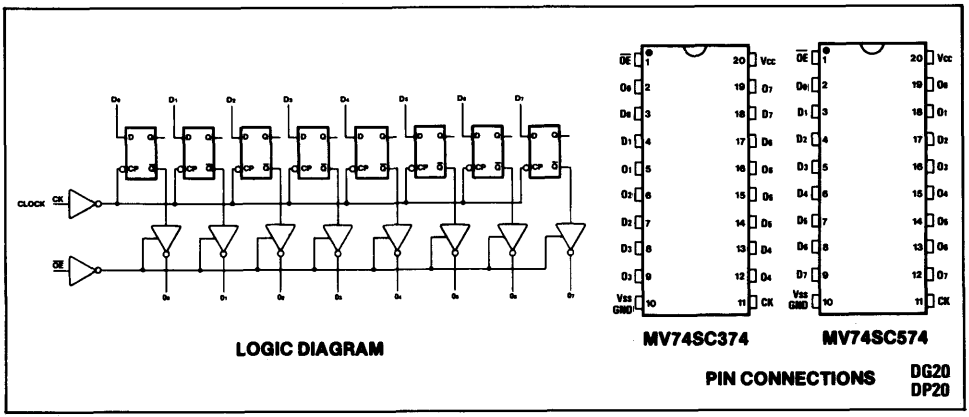


Fig.3 MV74SC374 and MV74SC574

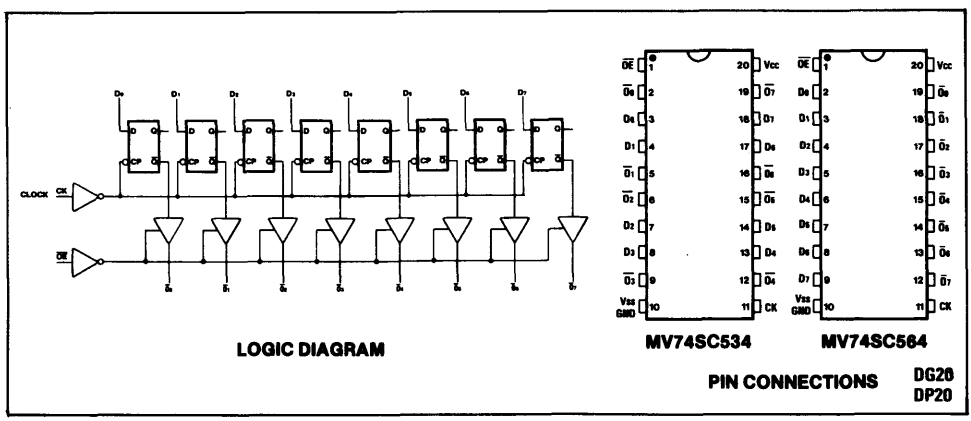


Fig.4 MV74SC534 and MV74SC564

RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{CC}	3	5	7	V
High level output current		I_{OH}		−24		mA
Low level output current		I_{OL}		24		mA
Operating free-air temperature		Tamb	0		70	°C
Width of clock/enable pulse,		t_w	20			nS
Data set up time	MV74SCXX3	t_{su}	15↓			nS
	MV74SCXX4		20↑			nS
Data hold time	MV74SCXX3	t_h	15↓			nS
	MV74SCXX4		15↑			nS

1. The arrow indicates clock/enable transition: ↑ LOW to HIGH, ↓ HIGH to LOW
2. Voltage values are with respect to V_{SS}/GND

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 0°C to +70°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
High level input voltage	V_{IH}	2.0			V	V_{CC} = 5.25V
Low level input voltage	V_{IL}			0.8	V	V_{CC} = 4.75V
Hysteresis ($V_T+ - V_T-$) $\overline{LE}$,CK,$\overline{OE}$			0.3		V	
High level output voltage	V_{OH}	2.4			V	V_{CC} = 4.75V, I_{OH} = -14mA
		4.0			V	I_{OH} = -3mA
Low level output voltage	V_{OL}			0.4	V	VCC = 4.75V, IOL = 10mA All other outputs high
Input current at maximum input voltage	I_I			15	μA	V_{CC} = 5.25V, V_I = 5.5V
High level input current any input	I_{IH}			10	μA	V_{CC} = 5.25V, V_I = 2.7V
Low level input current	I_{IL}			−10	μA	V_{CC} = 5.25V, V_I = 0.4V
Off-state output current high-level voltage applied	I_{OZH}			20	μA	V_{CC} = 5.25V, V_O = 2.7V
Off-state output current,low-level voltage applied	I_{OZL}			−20	μA	V_{CC} = 5.25V, V_O = 0.4V
Short circuit current (Note 3)	I_{OS}		−40		mA	V_{CC} = 5.25V
Quiescent supply current	I_{CC}			0.1	mA	V_{CC} = 5.25V, outputs disabled

3. Max. dissipation or 1mS duration should not be exceeded.
4. All TYP. values at Tamb = 25°C V CC = 5V

SWITCHING CHARACTERISTICS (Fig. 5)

Test conditions (unless otherwise stated):
V_{CC} = 5V, T_{amb} = +25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Propagation delay time, low-to-high level output	t_{PLH}		30 33	57 62	nS	MV74SC373, MV74SC573 MV74SC533, MV74SC563 C_L = 45pF
Propagation delay time high-to-low level output	t_{PHL}		30 33	56 59	nS	MV74SC374, MV74SC574 MV74SC534, MV74SC564 R_L = 667
Output enable time to low level	t_{PZL}		27	49	nS	C_L = 5 pF
Output enable time to high level	t_{PZH}		27	49	nS	
Output disable time from low level	t_{PLZ}		27	49	nS	R_L = 667
Output disable time from high level	t_{PHZ}		40	69	nS	
Operating frequency	f_{MAX}		20		MHZ	Note 5

5. Maximum clock frequency is tested with all outputs loaded.

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	VALUE
Supply voltage	V_{CC}	−0.5V to 7.0V
Input voltage	V_I	−0.3V to V_{CC} + 0.3V
Output current, per output	I_O	±75mA
Operating temperature	Tamb	−40°C to +85°C
Storage temperature	T_S	−65°C to 150°C
Package power dissipation	P	450mW

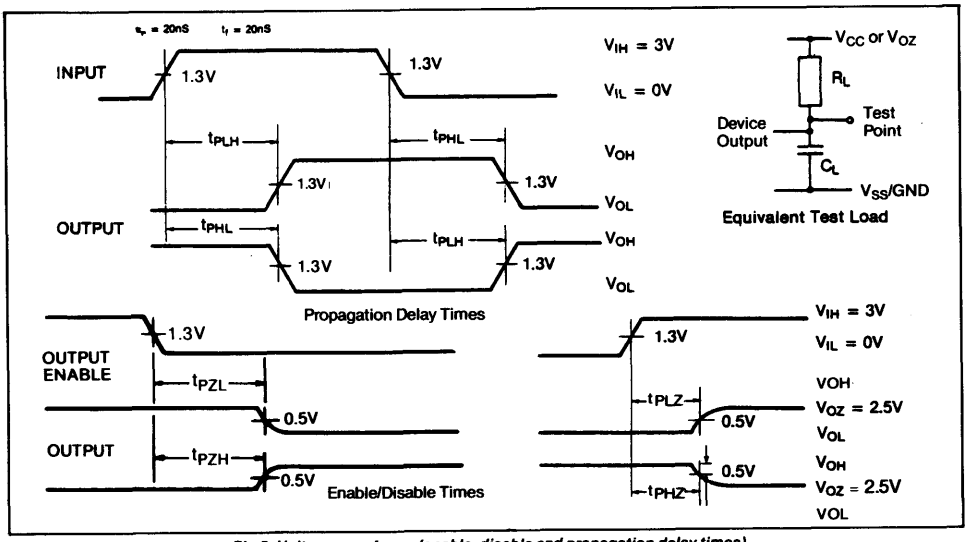


Fig.5 Voltage waveforms (enable, disable and propagation delay times)

PIN FUNCTIONS

Pin	Description
$D_{0\text{-}7}$	Data Inputs
$O_{0\text{-}7}$	Non Inverted Data Outputs
$\overline{O}_{0\text{-}7}$	Inverted Data Outputs
$\overline{OE}$	Output Enable
CK	Clock Input
$\overline{LE}$	Latch Enable
V_{CC}	Positive Supply Voltage
V_{SS}/GND	System Ground

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MV8860

DTMF DECODER

The MV8860 detects and decodes all 16 DTMF tone pairs. The device accepts the high group and low group square wave signals from a DTMF filter (MV8865) and provides a 3-state buffered 4-bit binary output. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost crystal as external components. The MV8860 is implemented in CMOS technology and incorporates an on-chip regulator, providing low power operation and power supply flexibility.

The MV8860 is available in Plastic DIL (DP) and Ceramic DIL (DG), both with an operating temperature range of −40°C to +85°C.

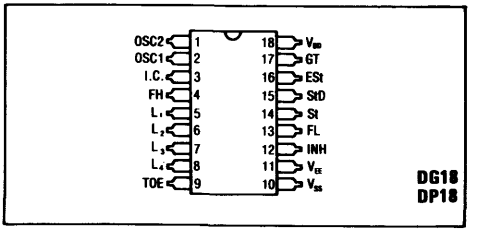


Fig.1 Pin connections (top view)

FEATURES

- 18 Pin DIL Package
- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times down to 20 ms
- Single Supply 5V, or 8 to 13 V Operation
- Latched 3-State Buffered Outputs
- Detects All 16 DTMF Combinations
- Uses Inexpensive 3.58 MHz Crystal
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times
- Equivalent to MT8860X

APPLICATIONS

In DTMF Receivers For:

- End-to-end Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

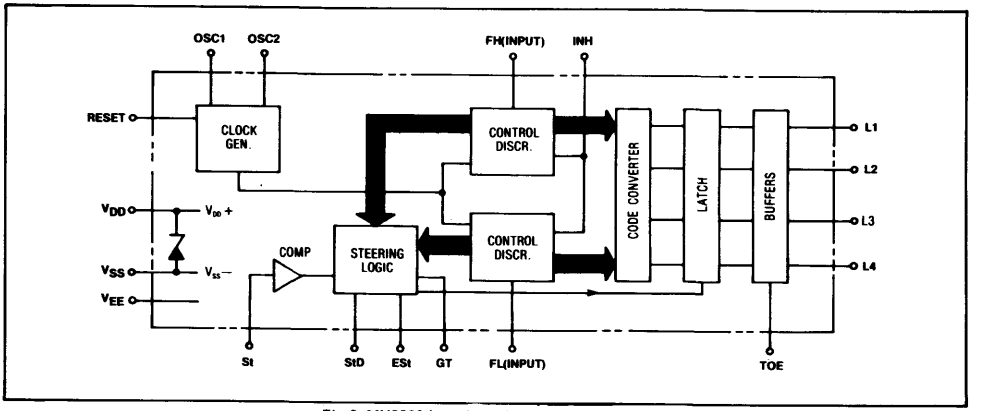


Fig.2 MV8860 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_c = 3.579545MHz
5V operation: $V_{DD} - V_{EE}$ = 5V, $V_{SS} = V_{EE}$, connections as Fig.5a
12V operation: $V_{DD} - V_{EE}$ = 12V, R_{SSEE} = 900Ω, connections as Fig.5b
Outputs not loaded
For input current parameters only, $V_{IH} = V_{IHO} = V_{DD}$, $V_{IL} = V_{EE}$, $V_{ILO} = V_{SS}$
All voltages referenced to V_{EE} unless otherwise noted.

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage ($V_{DD} - V_{EE}$)		V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2					8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage ($V_{DD} - V_{SS}$)		V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4					6.0	6.5	7.5	V	Connections Fig. 5b
5		Operating Supply Current		I_{DD}		1.3	4	mA	5V
6						2.5	5	mA	12V $V_{DD} - V_{SS}$ = 5.5V
7		Internal Logic Ground Pin Current		I_{SS}		5.5	6.7	mA	12V R_{SSEE} = 900Ω
8		Operating Power Consumption		P_O		6.5		mW	5V
9						66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)		V_{IH}	3.5	4		V	5V
11					8.5	9		V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)		V_{IL}		1	1.5	V	5V
13						3	3.5	V	12V
14		High Level Input Voltage OSC1		V_{IHO}	3.5	4.5		V	5V
15					10.5	11		V	12V
16		Low Level Input Voltage OSC1		V_{ILO}		0.5	1.5	V	5V Ref V_{SS}
17						0.5	1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage		V_{TSI}	2.04	2.27	2.5	V	5V
19					5.4	6.0	6.6	V	12V
20		Pull Down Sink Current (INH)		I_{IHI}	10	25	75	μA	5V
21					10	190	400	μA	12V
22		Pull Up Source Current (TOE)		I_{ILT}	2	7	45	μA	5V
23					10	55	250	μA	12V
24		Input High Leakage Current		I_{IH}		0.1	1.5	μA	5V or 12V
25		Input Low Leakage Current		I_{IL}		0.1	1.5	μA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)		V_{OH}	4.9			V	5V
27					11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)		V_{OL}			0.1	V	5V
29							0.1	V	12V
30		High Level Output Voltage OSC2		V_{OHO}	4.9			V	5V
31					11.9			V	12V
32		Low Level Output Voltage OSC2		V_{OLO}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.5V
35					0.5	0.8		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.5V
37					1.0	1.6		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OHO}	90	120		μA	5V V_{OH} = 4.5V
39					90	120		μA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OLO}	100	160		μA	5V V_{OL} = 0.5V
41					100	160		μA	12V V_{SS} = 0.5V
42		Tristate Output Current (High Impedance State)	$L_1 - L_4$ = H	I_{OZ}		0.035	1.5	μA	5V Appl V_{OL} = 0V
43			$L_1 - L_4$ = L			0.1	1.5	μA	5V Appl V_{OH} = 5V
44			$L_1 - L_4$ = H			0.1	1.5	μA	12V Appl V_{OL} = 0V
45			$L_1 - L_4$ = L			0.3	1.5	μA	12V Appl V_{OH} = 12V

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$; $V_{DD} = +5V$; $f_c = 3.579545MHz$

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions	
1	DETECTOR	Tone Frequency Deviation Accept		Δf_A			±2.5	% Nom.		
2		Tone Frequency Deviation Reject		Δf_R	±3.5			% Nom.		
3		Tone Present Detection Time		t_{DP}	6		10	ms		
4		Tone Absent Detection Time		t_{DA}	0.6	4	10	ms		
5		Guard Time (Adjustable)		$t_{GT(P\ or\ E)}$		20		ms	See Fig. 3	
6		Time to Receive = (t_{DP} + t_{GTP})		t_{REC}	28	30	35	ms	Fig. 7a R = 300k Ω	
7		Invalid Tone Duration (f_n of t_{REC})		$t_{\overline{REC}}$			20	ms	C = 0.1μF	
8		Interdigit Pause = (t_{DA} + t_{GTA})		t_{ID}	30			ms		
9		Acceptable Drop Out (f_n of t_{ID})		t_{DO}			20	ms		
10	I/P	FL FH Input Transition Time		t_T			1.0	us	10% - 90% V_{DD}	
11		Capacitance Any Input		C		5	7.5	pF		
12	OUTPUTS	Propogation Delay St to L_1 - L_4		t_{PL}		8	11	μs	V_{DD} 5V	
13						8	11	μs	V_{DD} 12V	
14		Propogation Delay St to StD		t_{PStD}		12	14	μs	V_{DD} 5V	
15						12	14	μs	V_{DD} 12V	
16		Propogation Delay TOE to L_1 - L_4	Enable	t_{PTE}		300		ns	V_{DD} 5V	
17						200		ns	V_{DD} 12V	
18			Disable	t_{PTD}		300		ns	V_{DD} 5V	
19						200		ns	V_{DD} 12V	
20	CLOCK	Crystal/Clock Frequency		f_c	3.5759	3.5795	3.5831	MHz	OSC 1	OSC 2
21		Clock Input (OSC 1)	Rise Time	t_{LHCI}			110	ns	10% - 90%	Externally
22			Fall Time	t_{HLCI}			110	ns	V_{DD} = V_{SS}	Applied
23			Duty Cycle	DC_{CI}	40	50	60	%		Clock
24		Clock Output (OSC 2)	Capacitive Load	C_{LOC}			30	pF	With Clock Drive to OSC 1	
25				C_{LOX}				nF	Sinusoidal Output With Crystal	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{EE}			16	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} −0.3	V_{DD} +0.3	V
Voltage OSC1 OSC2		V_{SS} −0.3	V_{DD} +0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	DP/DG Package	−40	+85	°C
Storage Temperature	DG Package	−55	+175	°C
	DP Package	−55	+125	°C

		Max
Power Dissipation	DG Package*	1000mW
	DP Package**	450mW

* Derate 16mW/°C above 75°C
** Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

Original Tone Character		TOE	L4	L3	L2	L1
	X	L	Z	Z	Z	Z
DR	1	H	L	L	L	H
	2	H	L	L	H	L
	3	H	L	L	H	H
	4	H	L	H	L	L
	5	H	L	H	L	H
	6	H	L	H	H	L
	7	H	L	H	H	H
	8	H	H	L	L	L
	9	H	H	L	L	H
	0	H	H	L	H	L
D	*	H	H	L	H	H
	#	H	H	H	L	L
	A	H	H	H	L	H
	B	H	H	H	H	L
	C	H	H	H	H	H
	D	H	L	L	L	L

(a) Output coding

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

(b) Inhibit function

ESt	St	GT	StD*
L	L	L	L
H	L	Z	L
L	H	Z	H
H	H	H	H

(c) Steering

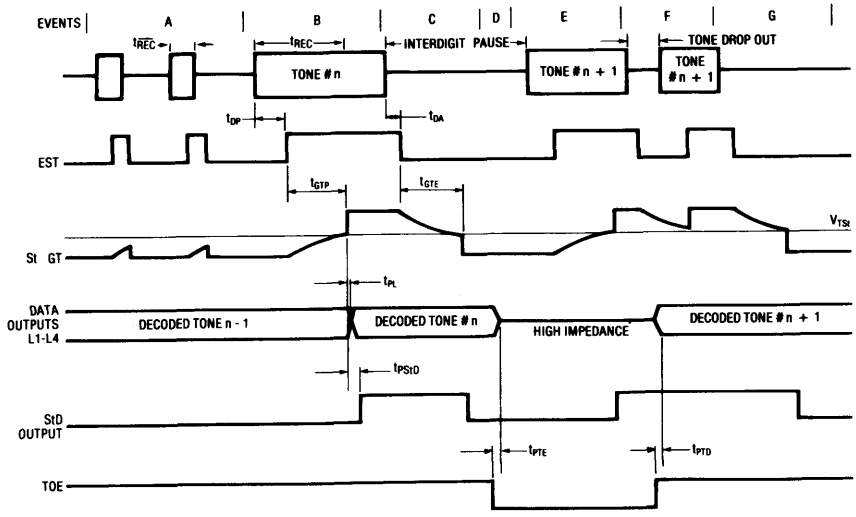
* DELAYED WRT St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH L = LOGIC LOW
Ø = "DON'T CARE" LOGIC HIGH OR LOW
Z = HIGH IMPEDANCE X = ANY CHARACTER

Table 1 Coding data



A) SHORT TONE BURSTS : DETECTED, TONE DURATION IS INVALID
B) TONE # n IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STAGE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n + 1 IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n + 1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n + 1 IS DETECTED AND VALIDATED.

Fig.3 Timing diagram

PIN FUNCTIONS

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5MΩ resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter	
5	L1	Data Outputs. 3 state buffered Provides 4 Bit binary word corresponding to the tone pair decoded, when enabled by TOE See Table 1 for state table	
6	L2		
7	L3		
8	L4		
9	TOE	3 state output enable input. Logic high on this input enables outputs L1-L4. Internal pull up	
10	V_{SS}	Internal logic ground. For $V_{DD} - V_{EE} = 5V$ V_{SS} connected to V_{EE}. For $V_{DD} - V_{EE} > 8V$, V_{SS} connected via resistor to V_{EE} see Fig. 5	
11	V_{EE}	Negative power supply. External logic ground	
12	INH	Inhibit input. Logic high inhibits detection of tones representing characters #, *, A, B, C, D. Internal pull down	
13	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter	
14	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage< V_{TSt} on this pin frees the device to accept a new tone pair. See Table 1c and Functional Description	
15	StD	Delayed Steering Output. Flags when a valid tone pair has been received. Presents logic high when output latch updated. When St voltage exceeds V_{TSt}. Returns to logic low when St voltage falls below V_{TSt}	
16	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low	
17	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Table 1c)	
18	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

OPERATING NOTES

The MV8860 is a CMOS Digital DTMF detector and decoder. Used in conjunction with a suitable DTMF filter (MV8865) it can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MV8860 must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sinewave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The high group and low group rectangular waves are applied to the MV8860s FH and FL inputs, respectively. The MV8865 DTMF filter provides these functions.

Within the MV8860 the FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Fig.2) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both high group and low group signals have been simultaneously detected, a flag ESt (Logic High), is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig.3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of 'tone absent' before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig.7a) is charged via resistor R from ESt which a DTMF tone pair is detected. After a period t_{GTP}, V_C exceeds the St input threshold voltage V_{TSt}, setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Table 1c) and timing diagram (Fig.3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents a 4 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs L_1 to L_4. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig.7a) falling below V_{TSt}.

Increasing the 'time to receive' (t_{REC}) tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig.7.

When L_1 to L_4 are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MV8860 may be operated from either a 5V or 8 to 13V supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig.5.

When using the MV8860 with the MV8865 DTMF filter it is only necessary to use the MV8865 crystal oscillator (see Fig.6). When using the higher supply voltage range the MV8865 OSC2 output should be capacitively coupled to the MV8860 OSC1 input as shown in Fig.6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

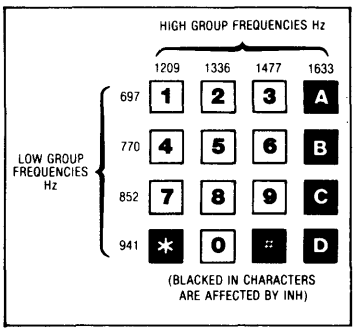


Fig.4 DTMF matrix, indicating character-tone pair correspondence

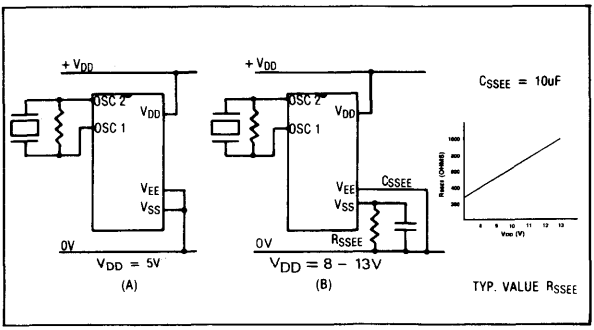
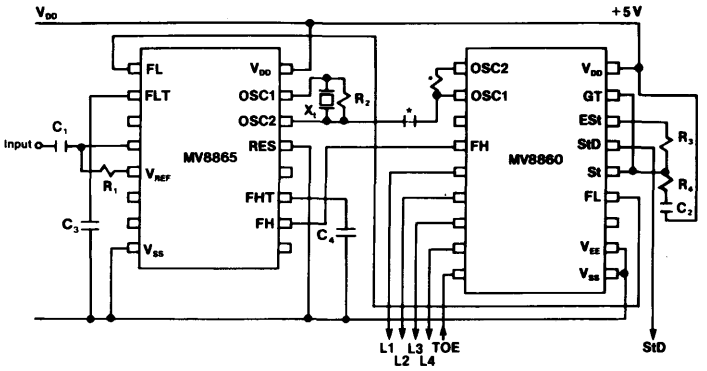


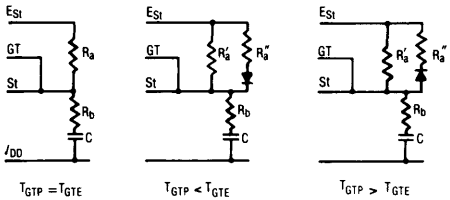
Fig.5 Power supply connection options



TYPICAL PERFORMANCE

DYNAMIC RANGE	30dB
TWIST	± 10dB
ACC. S/N RATIO	14dB
T_{REC}	30ms

Fig.6 Single-ended input receiver using the MV8865 (5V operation)



$$T_{GTP} = C(R_a + R_b) L_{ogn}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{DD} - V_{TSt}}\right)$$

$$T_{GTE} = C(R_a + R_b) L_{ogn}\left(\frac{R_a}{R_a + R_b}\right)\left(\frac{V_{DD} - V_{EE}}{V_{TSt}}\right)$$

FOR V_{OHESt}, V_{OLESt} Symetric About $V_{TSt} = \frac{1}{2} V_{DD}$
WITH $R_b < 0.1\ R_a$ $\quad R_b \geq V_{DD} - V_{EE}$ KΩ

$$R_b < 0.1\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$$

A) $T_{GTP} = T_{GTE} \triangleq 0.69\ R_a\ C\left(1 - \frac{R_b}{2R_a}\right)$

B) T_{GTP} $\triangleq 0.69\ C\left(\frac{R_a' R_a''}{R_a' + R_a''}\right)$

C) T_{GTE}

B) T_{GTE} $\triangleq 0.69\ R_a'\ C$

C) T_{GTP}

Fig.7 Guard time adjustment

PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

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MV8862/3

DTMF DECODER

The MV8862 and MV8863 each detect and decode all 16 DTMF tone pairs. The devices accept the high group and low group square wave signals from a DTMF FILTER (MV8865) and provide a 3 state buffered 8 Bit binary output with a choice of 3 coding formats. The two devices differ only in the specific output code formats they provide. The clock signals are derived from an on-chip oscillator requiring only a single resistor and low cost crystal as external components. The MV8862/3 is implemented in CMOS technology and incorporates an on chip regulator, providing low power operation and power supply flexibility.

The MV8862/3 are available in Plastic DIL (DP) and Ceramic DIL (DG), both with operating temperature range of −40°C to +85°C.

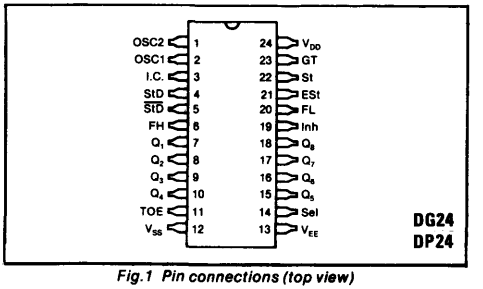


Fig.1 Pin connections (top view)

FEATURES

- Hex or 2 of 8 Output Codes
- Central Office Quality Detection
- Excellent Voice Talk-Off
- Detect Times down to 20 ms
- Single Supply 5 V, or 8 to 13 V Operation
- Latched 3-State Buffered Outputs
- Detects All 16 DTMF Combinations
- Uses Inexpensive 3.58 MHz Crystal
- Low Power CMOS Circuitry
- Adjustable Acquisition and Release Times
- Equivalent to MT8862/3X

APPLICATIONS

In DTMF Receivers For:

- End-to-end Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

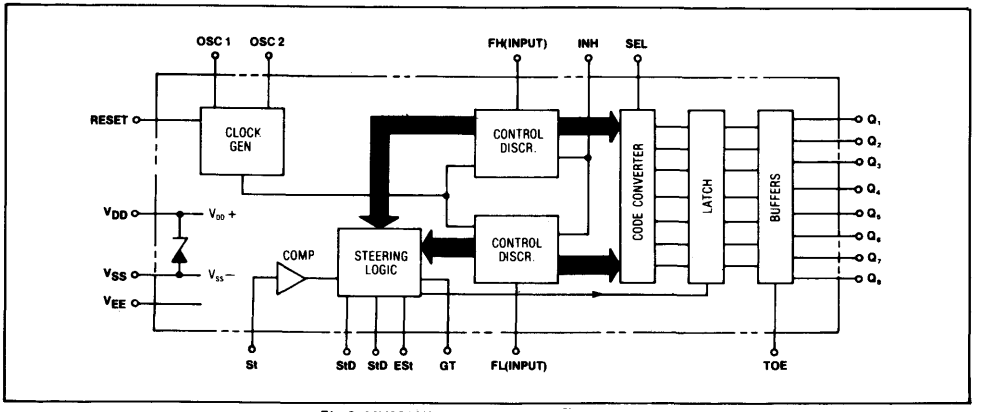


Fig.2 MV8862/3 functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_c = 3.579545MHz
5V operation: $V_{DD} - V_{EE}$ = 5V, $V_{SS} = V_{EE}$, connections as Fig.5a
12V operation: $V_{DD} - V_{EE}$ = 12V, R_{SSEE} = 900Ω, connections as Fig.5b
Outputs not loaded
For input current parameters only, $V_{IH} = V_{IHO} = V_{DD}$, $V_{IL} = V_{EE}$, $V_{ILO} = V_{SS}$
All voltages referenced to V_{EE}

		Characteristics		Symbol	Min	Typ	Max	Unit	Test Conditions
1	SUPPLY	Operating Supply Voltage (V_{DD} - V_{EE})		V_{DD}	4.75	5	5.25	V	Connections Fig. 5a
2					8		13	V	Connections Fig. 5b
3		Internal Logic Ground Voltage (V_{DD} - V_{SS})		V_{DDSS}	4.75		5.25	V	Connections Fig. 5a
4					6.0	6.5	7.5	V	Idd = 7mA
5		Operating Supply Current		I_{DD}		1.3	4	mA	5V
6						2.5	5	mA	12V V_{DD} - V_{SS} = 5.5V
7		Internal Logic Ground Pin Current		I_{SS}		5.52	6.7	mA	12V R_{SSEE} = 900Ω
8		Operating Power Consumption		P_o		6.5		mW	5V
9						66		mW	12V
10	INPUTS	High Level Input Voltage (All Inputs Except OSC1)		V_{IH}	3.5			V	5V
11					8.5			V	12V
12		Low Level Input Voltage (All Inputs Except OSC1)		V_{IL}			1.5	V	5V
13							3.5	V	12V
14		High Level Input Voltage OSC1		V_{IHO}	3.5			V	5V
15					10.5			V	12V
16		Low Level Input Voltage OSC1		V_{ILO}			1.5	V	5V Ref V_{SS}
17							1.5	V	12V Ref V_{SS}
18		Steering Input Threshold Voltage		V_{TSt}	2.04	2.27	2.5	V	5V
19					5.4	6.00	6.6	V	12V
20		Pull Down Sink Current (INH, Sel)		I_{SI}	10	25	75	µA	5V
21					10	190	400	µA	12V
22		Pull Up Source Current (TOE)		I_{SO}	2	7	45	µA	5V
23					10	55	250	µA	12V
24		Input High Leakage Current		I_{IH}		0.1	1.5	µA	5V or 12V
25		Input Low Leakage Current		I_{IL}		0.1	1.5	µA	
26	OUTPUTS	High Level Output Voltage (All Outputs Except OSC2)		V_{OH}	4.9			V	5V
27					11.9			V	12V
28		Low Level Output Voltage (All Outputs Except OSC2)		V_{OL}			0.1	V	5V
29							0.1	V	12V
30		High Level Output Voltage OSC2		V_{OH}	4.9			V	5V
31					11.9			V	12V
32		Low Level Output Voltage OSC2		V_{OL}			0.1	V	5V Ref V_{SS}
33							0.1	V	12V Ref V_{SS}
34		Output Drive Current (All Outputs Except OSC2)	P Channel Source	I_{OH}	0.4	0.6		mA	5V V_{OH} = 4.6V
35					0.5	0.8		mA	12V V_{OH} = 11.5V
36			N Channel Sink	I_{OL}	0.8	1.2		mA	5V V_{OL} = 0.4V
37					1.0	1.6		mA	12V V_{OL} = 0.5V
38		Output Drive Current OSC2	P Channel Source	I_{OH}	90	120		µA	5V V_{OH} = 4.6V
39					90	120		µA	12V V_{OH} = 11.5V
40			N Channel Sink	I_{OL}	100	160		µA	5V V_{OL} = 0.4V
41					100	160		µA	12V V_{SS} = 0.5V
42		Tristate Output Current (High Impedance State)	$Q_1 - Q_8$ = H	I_{OZ}		0.035	1.5	µA	5V Appl V_{OL} = 0V
43			$Q_1 - Q_8$ = L			0.10	1.5	µA	5V Appl V_{OH} = 5V
44			$Q_1 - Q_8$ = H			0.10	1.5	µA	12V Appl V_{OL} = 0V
45			$Q_1 - Q_8$ = L			0.30	1.5	µA	12V Appl V_{OH} = 12V

All "typical" parametric information is for design aid only, not guaranteed and not subject to production testing.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; V_{DD} = +5V; f_c = 3.579545MHz

		Characteristic	Symbol	Min	Typ*	Max	Unit	Test Conditions
1	DETECTOR	Tone Frequency Deviation Accept	Δf_A			± 2.5	% Nom.	
2		Tone Frequency Deviation Reject	Δf_R	± 3.5			% Nom.	
3		Tone Present Detection Time	t_{DP}	6		10	ms	
4		Tone Absent Detection Time	t_{DA}	0.6	4	10	ms	
5		Guard Time (Adjustable)	$t_{GT(P\ or\ E)}$		20		ms	See Fig.3
6		Time to Receive = (t_{DP} + t_{GTP})	t_{REC}	28	30	35	ms	Fig.7a R = 300kΩ
7		Invalid Tone Duration (f_n of t_{REC})	$t_{\overline{REC}}$			20	ms	C = 0.1μF
8		Interdigit Pause = (t_{DA} + t_{GTA})	t_{ID}	30			ms	
9		Acceptable Drop Out (f_n of t_{ID})	t_{DO}			20	ms	
10	I/P	FL FH Input Transition Time	t_T			1.0	μs	10% - 90% V_{DD}
11		Capacitance Any Input	C		5	7.5	pF	
12	OUTPUTS	Delay St to Q_1 - Q_8	t_{PL}		8	11	us	V_{DD} 5V or 12V
13								
14		Delay St to StD	t_{PStD}		12	14	μs	V_{DD} 5V or 12V
15		Synch. Delay Q_1 - Q_8 to StD	t_{QStD}		3.43		μs	
16		Propogation Delay TOE to Q_1 - Q_8 — Enable	t_{PTE}		300		ns	V_{DD} 5V
17					200		ns	V_{DD} 12V
18		Disable	t_{PTD}		300		ns	V_{DD} 5V
19					200		ns	V_{DD} 12V
20	CLOCK	Crystal/Clock Frequency	f_c	3.5759	3.5795	3.5831	MHz	OSC 1 OSC 2
21		Clock Input (OSC 1) — Rise Time	t_{LHCl}			110	ns	10% - 90% Externally
22		Fall Time	t_{HLCl}			110	ns	V_{DD} − V_{SS} Applied
23		Duty Cycle	DC_{Cl}	40	50	60	%	Clock
24		Clock Output (OSC 2) — Capacitive Load	C_{LO}			30		
25								

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max	
V_{DD} - V_{EE}			16	V
V_{DD} - V_{SS} (Low Impedance Supply)			5.5	V
Voltage on any pin except OSC1 OSC2		V_{EE} − 0.3	V_{DD} + 0.3	V
Voltage OSC1 OSC2		V_{SS} − 0.3	V_{DD} + 0.3	V
Max current at any pin (except V_{DD} & V_{EE})			10	mA
Operating Temperature	DP/DG Package	− 40	+ 85	°C
Storage Temperature	DG Package	−55	+175	°C
	DP Package	−55	+125	°C

		Max
Power Dissipation	DG Package*	1200mW
	DP Package**	600mW

* Derate 16mW/°C above 75°C
** Derate 6.3mW/°C above 25°C
All leads soldered to PC board.

Original Tone Character		TOE	Sel	8862								8863							
				Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_8	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1
	X	L	Ø	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
DR	1	H	L	L	L	L	H	L	L	L	H	L	L	L	L	L	L	L	H
	2	H	L	L	L	H	L	L	L	H	L	L	L	H	L	L	L	H	L
	3	H	L	L	L	H	L	L	H	L	H	L	H	L	L	L	H	L	H
	4	H	L	L	H	L	L	L	H	L	L	H	L	L	L	L	H	L	L
	5	H	L	L	H	L	L	H	L	L	H	H	L	H	L	L	H	L	H
	6	H	L	L	H	H	L	L	H	H	L	H	H	L	L	L	H	H	L
	7	H	L	L	H	H	H	L	H	H	H	L	L	L	H	L	H	H	H
	8	H	L	H	L	L	L	H	L	L	L	L	L	H	H	H	L	L	L
	9	H	L	H	L	L	H	H	L	L	H	L	H	L	H	H	L	L	H
	0	H	L	L	L	L	L	H	L	H	L	L	H	H	L	H	L	H	L
D	*	H	L	H	L	H	L	H	L	H	H	H	H	L	H	H	L	H	H
	#	H	L	H	L	H	H	H	H	L	L	H	L	L	H	H	H	L	L
	A	H	L	H	H	L	L	H	H	L	H	L	H	H	H	H	H	L	H
	B	H	L	H	H	L	H	H	H	H	L	H	L	H	H	H	H	H	L
	C	H	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H
	D	H	L	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
DR	1	H	H	H	H	H	L	H	H	H	L	L	L	L	H	L	L	L	H
	2	H	H	H	H	L	H	H	H	H	L	L	L	H	L	L	L	L	H
	3	H	H	H	L	H	H	H	H	H	L	L	H	L	L	L	L	L	H
	4	H	H	H	H	L	H	H	H	L	H	L	L	L	H	L	L	H	L
	5	H	H	H	H	L	H	H	H	L	H	L	L	H	L	L	L	H	L
	6	H	H	H	L	H	H	H	L	H	H	L	H	L	L	L	L	H	L
	7	H	H	H	H	H	L	H	L	H	H	L	L	L	H	L	L	H	L
	8	H	H	H	H	L	H	H	L	H	H	L	L	H	L	L	H	L	L
	9	H	H	H	L	H	H	H	L	H	H	L	H	L	L	L	H	L	L
	0	H	H	H	H	H	L	H	L	H	H	L	L	H	L	H	L	L	L
D	*	H	H	H	H	H	L	L	H	H	H	L	L	L	H	H	L	L	L
	#	H	H	H	L	H	H	H	L	H	H	L	H	L	L	H	L	L	L
	A	H	H	L	H	H	H	H	H	H	L	H	L	L	L	L	L	L	H
	B	H	H	L	H	H	H	H	H	L	H	H	L	L	L	L	L	H	L
	C	H	H	L	H	H	H	H	L	H	H	H	L	L	L	L	H	L	L
	D	H	H	L	H	H	H	L	H	H	H	H	L	L	L	H	L	L	L

(a) Output coding

Detected Character	INH	ESt
None	Ø	L
X	L	H
DR	H	H
D	H	L

(b) Inhibit function

ESt	St	GT	StD*	$\overline{StD}$*
L	L	L	L	H
H	L	Z	L	H
L	H	Z	H	L
H	H	H	H	L

(c) Steering

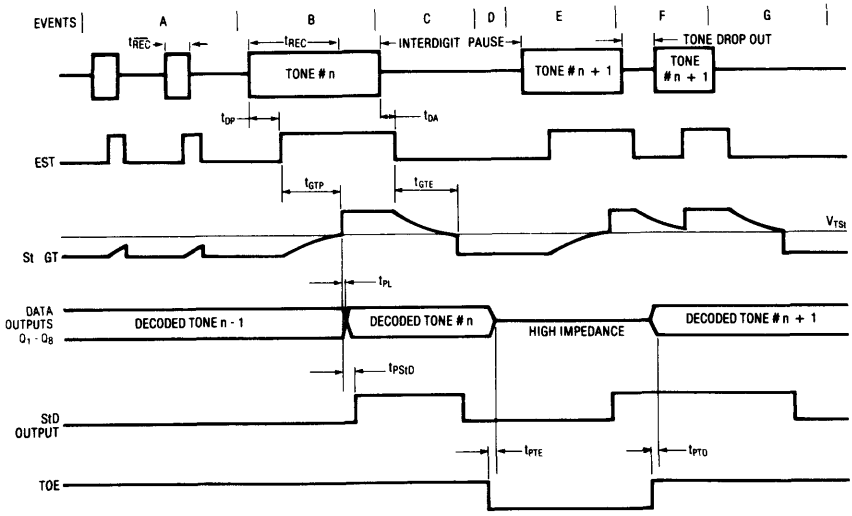
* DELAYED FROM St.

FOR THE PURPOSE OF THESE TABLES CONSIDER:

$V_{St} < V_{TSt}$ LOGIC LOW (L)
$V_{St} > V_{TSt}$ LOGIC HIGH (H)

H = LOGIC HIGH
X = ANY CHARACTER
L = LOGIC LOW
Z = HIGH IMPEDANCE
Ø = "DON'T CARE" LOGIC HIGH OR LOW

Table 1 Coding data



A) SHORT TONE BURSTS : DETECTED, TONE DURATION IS INVALID
B) TONE # n IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
C) END OF TONE # n IS DETECTED AND VALIDATED.
D) 3 STAGE OUTPUTS DISABLED (HIGH IMPEDANCE).
E) TONE # n + 1 IS DETECTED, TONE DURATION IS VALID, DECODED TO OUTPUTS.
F) TRISTATE OUTPUTS ARE ENABLED. ACCEPTABLE DROP OUT OF TONE # n + 1 DOES NOT REGISTER AT OUTPUTS.
G) END OF TONE # n + 1 IS DETECTED AND VALIDATED.

Fig.3 Timing diagram

PIN FUNCTIONS

Pin	Name	Description	
1	OSC2	CLOCK OUTPUT	3.58MHz crystal with parallel 5M Ω resistor connected between these pins completes internal oscillator, running between V_{DD} and V_{SS}.
2	OSC1	CLOCK INPUT	
3	IC	Internal connection for testing only (reset) Note 1	
4	StD	Delayed Steering Output. Flags when a valid tone pair has been received. When the St voltage exceeds V_{TSt}, the output latch is updated, then StD presents a logic high. Returns to logic low when St voltage falls below V_{TSt}. (See Table 1c)	
5	$\overline{StD}$	Inverted StD.	
6	FH	High frequency group input. Accepts single rectangular wave High group tone from DTMF filter.	
7	Q1	Data outputs 3 state buffered.	
8	Q2	Provides 4 bit binary word (Sel. low) or half of 2 of 8 binary word (Sel. high), corresponding to the tone pair decoded, when enabled by TOE.	
9	Q3		
10	Q4	See Table 1 for state table.	
11	TOE	3 state output enable input. Logic high on this input enables outputs Q1-Q8. Internal pull up	
12	V_{SS}	Internal logic ground. For $V_{DD} - V_{EE} = 5V$, V_{SS} connected to V_{EE}. For $V_{DD} - V_{EE} > 8V$, V_{SS} connected via resistor to V_{EE} see Fig. 5	
13	V_{EE}	Negative power supply. External logic ground.	
14	Sel.	Output Code Select. Logic low on this pin selects Q1-Q4, Q5-Q8 to provide 2 different 4 bit binary output codes. A logic high selects Q1-Q8 to provide a 2 of 8 output code (See Fig. 2).	
15	Q5	Data outputs 3 state buffered.	
16	Q6	Provides 4 bit binary word (Sel. low) or half of 2 of 8 binary word (Sel. high), corresponding to the tone pair decoded, when enabled by TOE.	
17	Q7		
18	Q8	See Table 1 for state table.	
19	Inh	Inhibit input. Logic high inhibits detection of tones (D tones in Table 1a) representing characters #, *, A, B, C, D. Internal pull down.	
20	FL	Low frequency group input. Accepts single rectangular wave low group tone from DTMF filter.	
21	ESt	Early Steering Output. Presents a logic high immediately the digital algorithm detects a recognisable tone pair. Any momentary loss of the incoming tone or excessive distortion of the tone will cause ESt to return to a logic low.	
22	St	Steering input. A voltage greater than V_{TSt} on this input causes the device to accept validity of the detected tone pair and latch the corresponding codeword at the outputs Voltage less than V_{TSt} on this pin frees the device to accept a new tone pair. See Table 1c and Functional Description.	
23	GT	Guard Time Output. 3 state output. Normally connected to St, is used in the steering algorithm and is a function of St and ESt (See Table 1c)	
24	V_{DD}	Positive power supply	

Note 1: Must be left open circuit.

OPERATING NOTES

The MV8862 is a CMOS Digital DTMF Detector and Decoder. The MV8863 is an identical device except that it provides a different set of output codes. The codes of the MV8863 are the same as those provided by MV8820. Used in conjunction with a suitable DTMF filter (MV8865) the MV8862 or MV8863 can detect and decode all 16 Standard DTMF tone pairs, accurately discriminating between adjacent frequencies in both high and low groups in the presence of noise and normal voice signals.

To form a complete DTMF receiver the MV8862(3) must be preceded by a DTMF filter, the function of which is to separate the high group and low group components of the composite dual tone signal and limit the resulting pair of sinewave signals to produce rectangular wave signals having the same frequencies as the individual components of the composite DTMF input. The high group and low group rectangular waves are applied to the MV8862(3)s FH and FL inputs respectively. The MV8865 DTMF Filter provides these functions.

Within the MV8862(3) FL and FH signals are operated on by a complex averaging algorithm. This is implemented using digital counting techniques (Control/Discriminators, Fig.2) to determine the frequencies of the incoming tones and verify that they correspond to standard DTMF frequencies. When both high group and low group signals have been simultaneously detected, a flag ESt (Logic High), is generated. ESt is generated (cancelled) rapidly on detecting the presence (absence) of a DTMF tone pair (see Fig.3) and is used to perform a final validity check.

The final validity check requires the input DTMF signal to be present uninterrupted by drop out or excessive distortion (which would result in ESt being cancelled) for a minimum time (t_{REC}) before being considered valid. This contributes greatly to the talk off performance of the system. The check also imposes a minimum period of 'tone absent' before a valid received tone is recognised as having ended. This allows short periods of drop out (t_{DO}) or excessive noise to occur during a received tone, without it being misinterpreted as two successive characters by the steering circuit (ESt, St, GT). A capacitor C (Fig.7a) is charged via resistor R from ESt which a DTMF tone pair is detected. After a period t_{GTP}, V_C exceeds the St input threshold voltage V_{TSt}, setting an internal flag indicating the detected signal is valid. Functioning of the check algorithm is completed by the three state output GT which is normally connected to St and operates under the control of ESt and St. Its mode of operation is shown by the steering state table (Table 1c) and timing diagram (Fig.3).

Internally the presence of the ESt flag allows the control/discriminator to identify the detected tones to the code converter which in turn presents an 8 bit binary code word, corresponding to the original transmitted character, to the output latch. The appearance of the internal St flag clocks the latch, presenting the output code at the tristate outputs Q_1 to Q_8. The St internal flag is delayed (by t_{PStD}) and appears at the StD output to provide a strobe output function indicating that a new character has been received and the output updated. StD will return to a logic low after the St flag has been reset by V_C (Fig.7a) falling below V_{TSt}.

Increasing the 'time to receive' (t_{REC}) tends to further improve talk off performance (discrimination against voice simulation of a DTMF tone pair) but degrades the acceptable signal to noise ratio for the incoming signal. Increasing interdigit pause t_{ID} further reduces the probability of receiving the same character twice and improves acceptable signal to noise ratio but imposes a longer interdigit pause. Reducing t_{REC} or t_{ID} has the opposite effect respectively. The values of t_{REC} and t_{ID} can be tailored by adjusting t_{GTP} and t_{GTA} as shown in Fig.7.

When $Q_1 - Q_8$ are connected to a data bus TOE may be controlled by external circuitry or connected directly to StD automatically enabling the outputs whenever a tone is received. In either case StD may be used to flag external circuitry indicating a character has been received.

The MV8862(3) may be operated from either a 5V or 8 to 13V supply by use of the internal zener reference. The relevant connection diagrams are shown in Fig.5.

When using the MV8862(3) with the MV8865 DTMF Filter it is only necessary to use the MV8865 crystal oscillator (see Fig.6). When using the higher supply voltage range the MV8865 OSC2 output should be capacitively coupled to the MV8862(3) OSC1 input as shown in Fig.6.

Where it is desirable to receive only the characters available on a rotary dial telephone, taking INH to a logic high inhibits detection of the additional DTMF characters. Incidentally this also further improves talk off due to the reduced number of detectable tones.

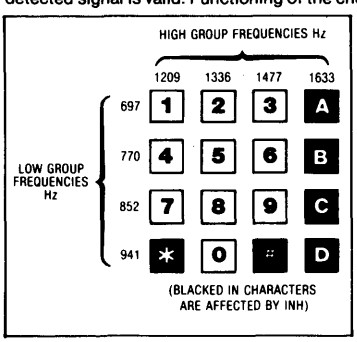


Fig.4 DTMF matrix, indicating character-tone pair correspondence

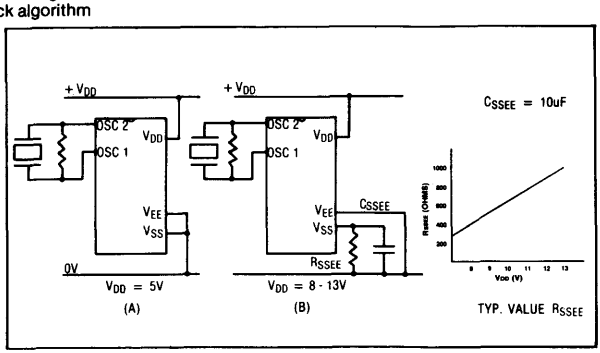


Fig 5 Power supply connection options

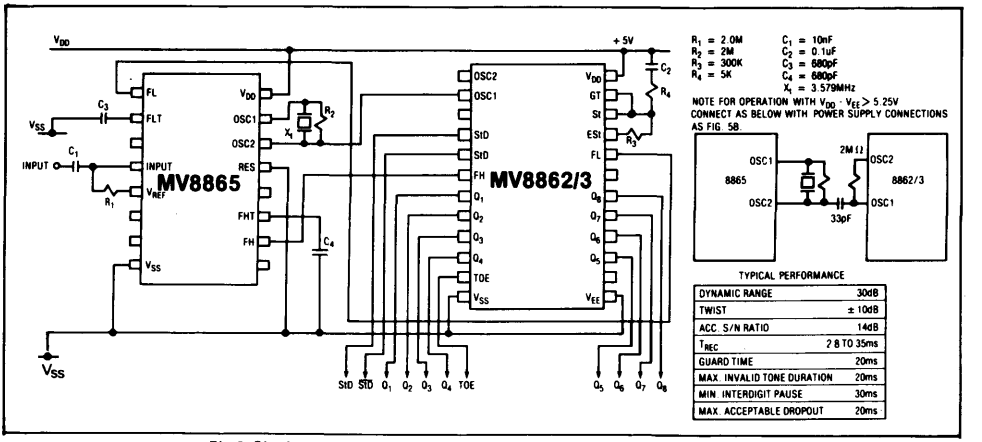


Fig.6 Single-ended input receiver using the MV8865 (5 V operation)

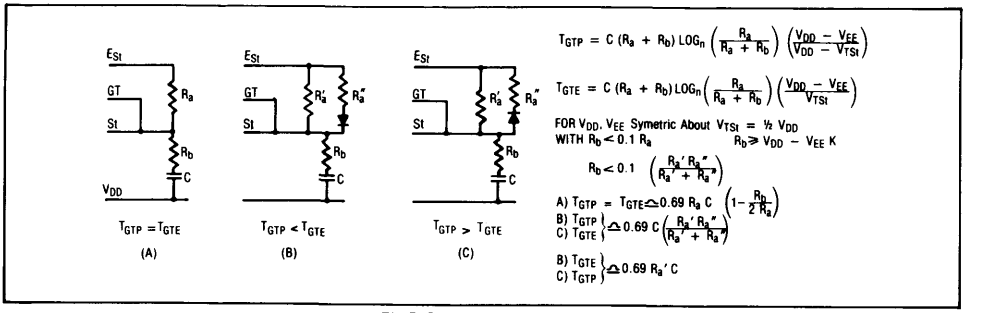


Fig.7 Guard time adjustment

PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV8865

DTMF FILTER

The MV8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a DTMF Digital Detector (i.e. MV8860/62/63). Switched capacitor techniques are used to implement the filters and the device is fabricated using Plessey Semiconductors' high density ISO/CMOS technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as an external component. The MV8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

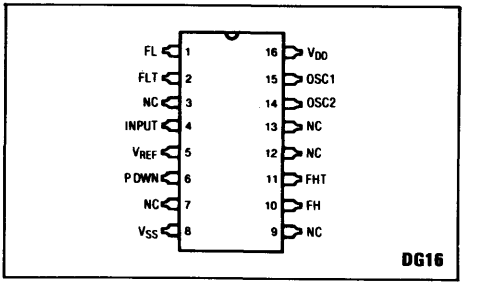


Fig.1 Pin connections (top view)

FEATURES

- Provides DTMF High and Low Group Filtering
- Hard Limiting on Filter Outputs
- 6 Pole Band Pass High and Low Group Filters
- 38 dB Intergroup Attenuation
- Dial Tone Suppression
- +5 to +12 V Single Supply Operation
- Logical Power Down
- Uses Inexpensive 3.58 MHz Crystal
- Wide Dynamic Range 30 dB
- Equivalent to MT8865X

APPLICATIONS

In DTMF Receivers for:

- End to End Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

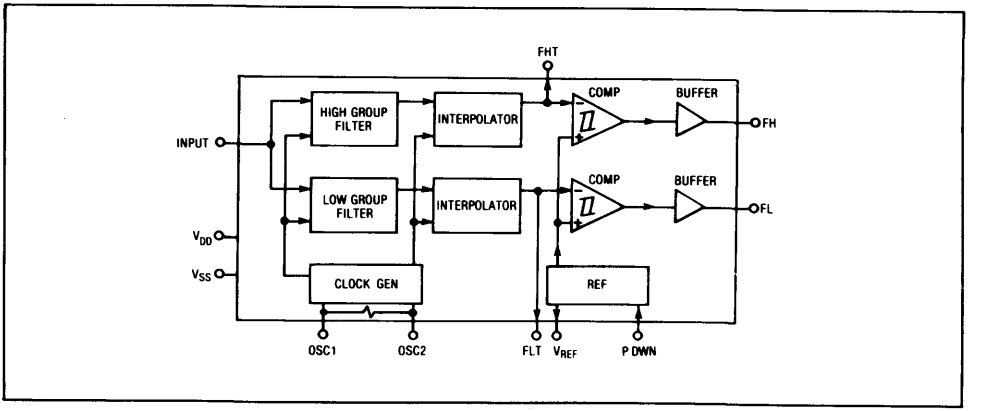


Fig.2 MV8865X functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_{CLK} = 3.579545 MHz
All voltages wrt V_{SS}

		Characteristic		Symbol	V_{DD} = 5V			V_{DD} = 12V			Unit	Test Conditions	
					Min	Typ	Max	Min	Typ	Max			
1	SUPPLY	Operating Supply Voltage		V_{DD}	4.75					13	V		
2		Operating Supply Current		I_{DD}		1.2	2.5		5	7.5	mA	PDWN = V_{SS}	
3		Standby Supply Current		I_{DDS}		100	150		300	400	µA	PDWN = V_{DD}	
4		Operating Power Consumption		P_O		6			60		mW	PDWN = V_{SS}	Fig. 6(c)
5		Standby Power Consumption		P_S		0.5			1.5		mW	PDWN = V_{DD}	C = 15pF
6	INPUTS	Low Level Input Voltage	PDWN & OSC 1	V_{IL}			1.5			3.5	V		
7		High Level Input Voltage		V_{IH}	3.5			8.5			V		
8		Pull Down Sink Current	PDWN	I_{IH}		3	6		12	24	µA		
9		Input Current	OSC 1	I_I		±2.5			±6		µA		
10	OUTPUTS	Low Level Output Voltage	FL, FH	V_{OL}			0.1			0.1	V	No load	
11		High Level Output Voltage	OSC 2	V_{OH}	4.9			11.9			V		
12		Output Drive Current — Sink	N Channel FL, FH	I_{OL}	0.2			0.5			mA	V_{OL} = 0.4V (5V)	
13			OSC 2		0.1			0.25			mA	V_{OL} = 1.2V (12V)	
14		Source	P Channel FL, FH	I_{OH}	0.2			0.5			mA	V_{OH} = 4.6V (5V)	
15			OSC 2		0.1			0.25			mA	V_{OH} = 10.8V (12V)	

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max		Parameter		Max
V_{DD} - V_{SS}			15	V	Power Dissipation	DG package[1]	850mW
Voltage on any pin		V_{SS} - 0.3	V_{DD} + 0.3	V			
Max. current at any pin			10	mA	[1]Derate 16mW/°C above 75°C		
Operating Temperature		40°C	+85	°C			
Storage Temperature	DG package	−65°C	+150	°C			

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
t_{amb} = +25°C; f_c = 3.579545 MHz; V_{DD} = 4.75 V to 13 V

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions	
1	FILTER	Dynamic Range			30		36	dB		
2		Valid Input Signal Levels					$V_{DD}/2$	V_{pp}		
3		(Each tone of composite signal)			27.9		883	mVrms	V_{DD} = 5V	
4					0.134		4.242	Vrms	V_{DD} = 12V	
5		Input Impedance		Z_I	10			MΩ		
6		Low Group Sensitivity (1)			-28.85			dBm	V_{DD} = 5V	
7		Low Group Sensitivity (1)			-21.25			dBm	V_{DD} = 12V	
8		High Group Sensitivity (1)			-28.85			dBm	V_{DD} = 5V	
9		High Group Sensitivity (1)			-21.25			dBm	V_{DD} = 12V	
10		Intergroup	Low Group with	IR_{L1209}	40	45		dB	1209Hz	w.r.t.
11			High Tone	IR_{L1477}	36	40		dB	1477Hz	770Hz
12		Rejection	High Group with	IR_{H941}	40	45		dB	941Hz	w.r.t.
13			Low Tone	IR_{H770}	36	40		dB	770Hz	1336Hz
14		Dial Tone	Low Group	DR_{L440}		60		dB	440Hz	w.r.t
15				DR_{L350}		30		dB	350Hz	770Hz
16		Rejection	High Group	DR_{H440}		60		dB	440Hz	w.r.t.
17				DR_{H350}		50		dB	350Hz	1336Hz
18		FHT FLT Maximum Permissible Load		R_{LFT}	250			KΩ		
19				C_{LFT}			2000	pF		
20	LIM	Output Rise Time	FL, FH	t_{TLHO}		90	150	ns	10% to	
21		Output Fall Time		t_{THLO}		60	100	ns	90% V_{DD}	
22	CLOCK	Crystal/Clock Freq.	OSC 1, OSC 2	f_c	3.5759	3.5795	3.5831	MHz		
23		Clock	Rise Time	t_{LHCI}			110	ns	10% to	Externally
24		Input	Fall Time	t_{HLCI}			110		90% V_{DD}	Applied
25		(OSC 1)	Duty Cycle	DC_{CI}	40	50	60	%		Clock
26		Clock Output OSC 2	Capacitive Load	C_{LOC}			30	pF	Unbalanced load, see Operating Notes	
27		Capacitance Any Input		C_i		5	7.5	pF		

NOTES
1. The sensitivity characteristic specifies correct operation of the post-comparator outputs at minimum input signal levels. It is valid for each of the four DTMF tones in each passband.

PIN FUNCTIONS

DIP Pin	Name	Description	
1	FL	Low group limiter output.	
2	FLT	Test output. Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.	
3	NC	Not connected.	
4	INPUT	Tone signal input (single ended).	
5	V_{REF}	Internal reference, can be used to bias input via 2MΩ resistor.	
6	PDWN	Power down active high. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.	
7	NC	Not connected.	
8	V_{SS}	Negative (0V) power supply.	
9	NC	Not connected.	
10	FH	High group limiter output.	
11	FHT	Test output. Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.	
12	NC	Not connected.	
13	NC	Not connected.	
14	OSC 2	Clock Output.	3.58MHz crystal connected between these pins completes internal oscillator.
15	OSC 1	Clock Input.	
16	V_{DD}	Positive power supply.	

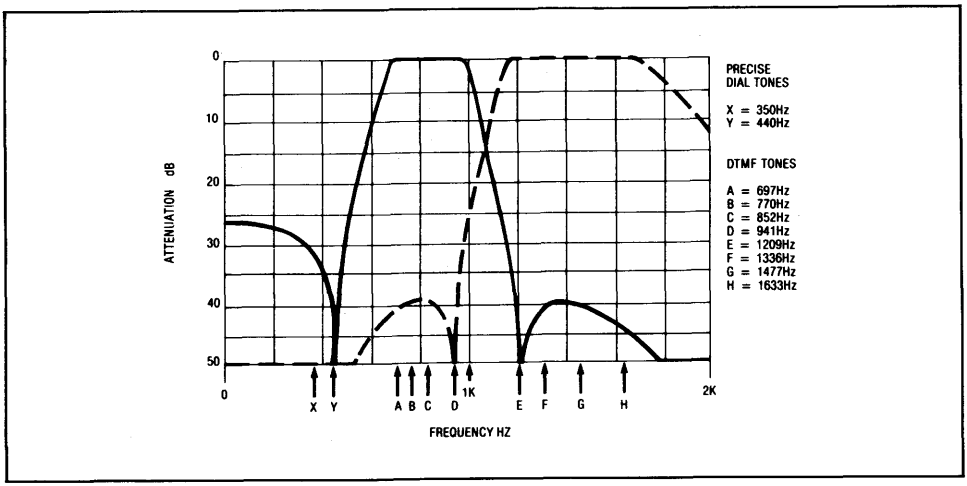


Fig.3 Typical filter characteristics

OPERATING NOTES

The MV8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of one of Plessey Semiconductors' range of DTMF Digital Decoders (MV8860/62/63), see Fig.4.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor band-pass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig.3) also incorporates a notch at 440 Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting.

The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MV8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig.4) or via a differential buffer to a telephone line (Fig.5). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input capacitively coupled, this is achieved by connecting the signal input to V_{REF} (Pin 5) via a 2 MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680 pF capacitors.

Unbalanced Loads

Presenting a high unbalanced capacitive load to the oscillator crystal can cause Attenuation of the oscillator output signal and increased supply current (see Fig.6). Where the MV8865 oscillator is required to drive a high capacitive load such as a number of other MV8865/8860s it is desirable to connect a capacitor between OSC1 and V_{SS}, the value of this capacitor being equal to the capacitive loading at OSC2.

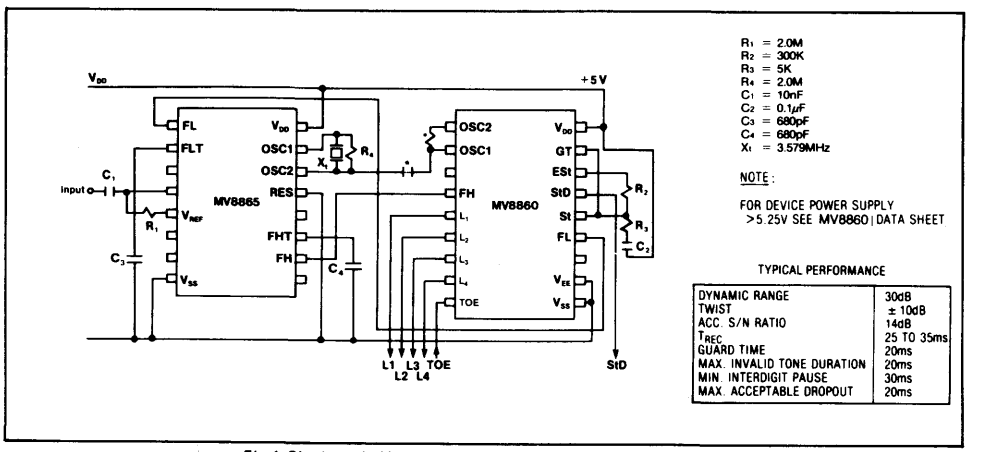


Fig.4 Single-ended input receiver using the MV8860 (5 V operation)

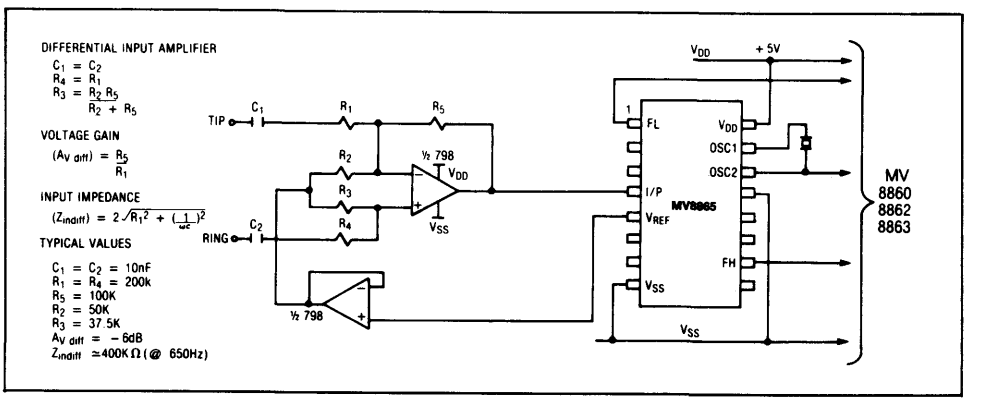


Fig.5 Connection to a telephone line

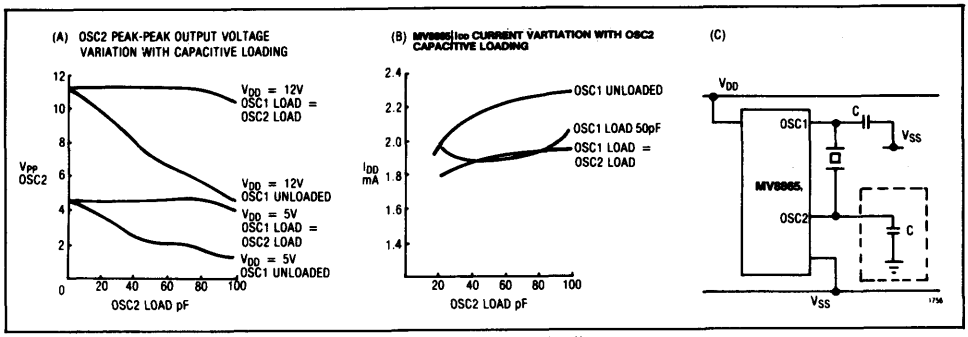


Fig.6 Crystal oscillator loading

PLESSEY
Semiconductors

SL650B & C SL651B & C

MODULATOR/PHASE LOCKED LOOP CIRCUITS FOR MODEMS

The SL650/1 are versatile integrated circuits capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using the SL650 or SL651, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage –, current –, or resistance – programmable from zero to greater than 10,000.

An auxiliary amplifier with a voltage gain of, typically, 5000 is incorpated in the SL650 for use when it is required to interface to specified levels and impedances. The auxiliary amplifier features low bias current (typically 25nA), fast recovery from overload, and a short-circuit output current of ±7.5mA.

The auxiliary amplifier is omitted from the SL651.

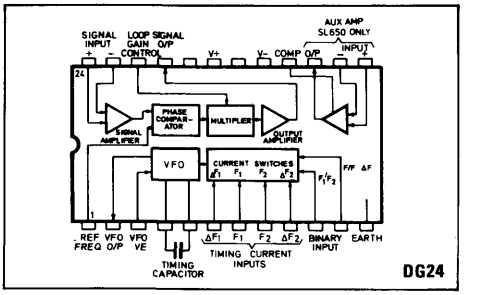


Fig.1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100:1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient:
  'B' Types 20 ppm/°C Max.
  'C' Types 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface
- Phase Comparator O/P Can Swing to Supply Voltages
- On-Chip Auxiliary Amplifier (SL650)

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	–55°C to +125°C

ELECTRICAL CHARACTERSTICS

Test conditions (unless otherwise stated)
Supply voltage ±6V
Temperature T_A +22°C ±2°C)

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current I_{CC}	17, 19			3	mA	
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	17, 19		±20		ppm/%	
Voltage at timing current inputs	6, 7, 8, 9		±10		mV	See note 2
VFO output, 'low' state	2		0	0.2	V	
VFO output, 'high' state	2	+1.1	+1.3		V	$R_L \geqslant 10k\Omega$
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	10, 11			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	10, 11	+2.4			V	
Input current	10, 11		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	23, 24		±2		mV	V_{out} = 0V
Input bias current	23, 24		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	23, 24		100		kΩ	
Common mode I/P voltage range	23, 24	±4			V	
Differential I/P to limit (AC)	23, 24		1.0	10	mV rms	See note 4
Output current	21, 22	±1.0	±2.0	±5.0	mA	I_{22} = 250μA
Current gain (pin 22 to pin 21)	21, 22	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	21,23,24	±100	±250		mA/V	See note 5
Output voltage, linear range	21	±5	±5.5		V	
Output current	21			±2	μA	I_{22} = 0
Phase comparator I/P 'low'	1	−4		−0.2	V	
Phase comparator I/P 'high'	1	+1.9		+5.3	V	
Auxiliary amplifier (SL650 only)						
Differential I/P offset voltage	13, 14		±2		mV	V_{out} = 0V
Input bias current	13, 14		0.025	0.5	μA	V_{in} = 0V
Differential I/P resistance	13, 14	0.2	3		MΩ	
Common mode I/P voltage range	13, 14	±4			V	
Voltage gain (13–14) to 15	13,14,15	1000	5000		–	
Output voltage range	15	±4	±4.8		V	$R_L \geqslant 2k\Omega$
Output current limit	15	±4	±6.5	±12	mA	

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL650C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin 21) voltage-limits first.
5. For a control current input to pin 22 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	± 7.5V
Storage temperature	−55° to +175°C
Operating temperature	−55° to +125°C
Input voltages	Not greater than supplies

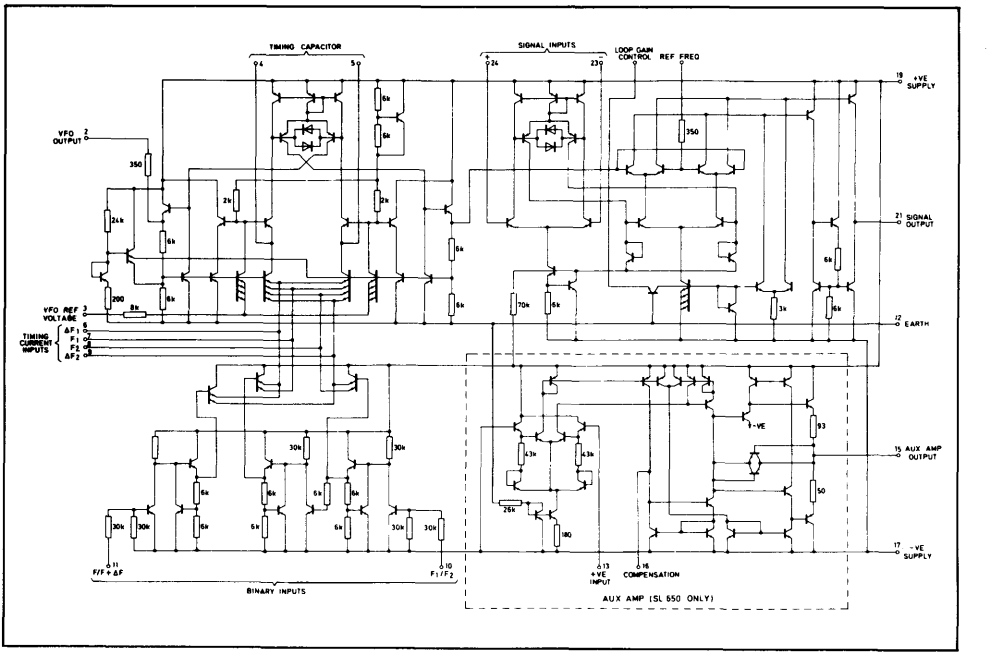


Fig. 2 Circuit diagram of SL650/SL651

OPERATING NOTES

Basic VFO Relationships

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 4 and 5, and directly proportional to the VFO timing current (see Fig.3). Four current switches, controlled by TTL-compatible logic inputs on pins 10 and 11 select a combination of external resistors (connected to pins 6, 7, 8 and 9) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to 0V however, then only the current switch associated with pin 7 is closed. the VFO timing current is then determined solely by the value of one resistor (R2 in Fig.3), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig.4 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR} \cdot \frac{V_R}{V_3}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 3), then

$$V_R = V_3$$

$$\text{and } f = \frac{1}{CR}$$

Pin 3 is normally connected to the chip negative supply; if, however, pin 3 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR} \cdot \frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 3

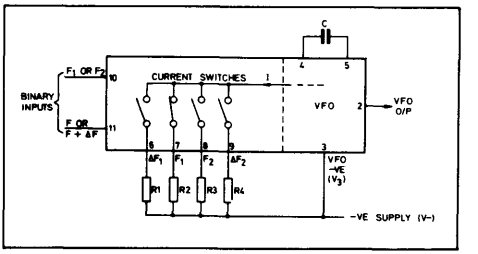


Fig. 3 VFO and binary interface

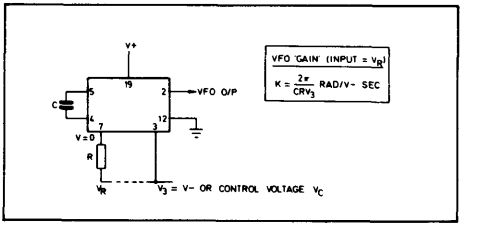


Fig. 4 VFO basic configuration

The timing current I should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig.3 the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 10	Pin 11	Timing Pins	VFO Frequency
LO	LO	7	$\frac{1}{CR_2}$
LO	HI	6 & 7	$\frac{1}{CR_2} + \frac{1}{CR_1}$
HI	LO	8	$\frac{1}{CR_3}$
HI	HI	8 & 9	$\frac{1}{CR_3} + \frac{1}{CR_4}$

Table 1 Binary interface relationships

Auxiliary amplifier

Internal compensation provides stability down to a closed loop gain of typically 20dB. A 30pF capacitor connected between pins 16 and 15 will give compensation down to a closed loop gain of unity. The output is short circuit protected but is not recommended for driving loads less than 2k

Phase Comparator

The phase comparator parameters are defined as follows (see Fig.5):

$$\text{Overall transconductance} = \frac{I_{21}}{V_{24} - V_{23}}$$

$$\text{Overall voltage gain} = \frac{V_{21}}{V_{24} - V_{23}}$$

The input amplifier will limit when the peak input ($V_{24} - V_{23}$) exceed ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

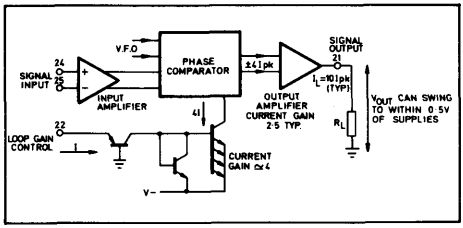


Fig. 5 Phase comparator

PLESSEY
Semiconductors

SL652C

MODULATOR/PHASE LOCKED LOOP

The SL652C is a versatile integrated circuit capable of performing all the common modulation functions (AM, PAM, SCAM, FM, FSK, PSK, PWM, tone-burst, delta-modulation, etc.). A wide variety of phase-locked loops can be realised using this device, with all parameters accurately controllable; they can also be used to generate precise waveforms at frequencies up to 0.2MHz.

The highly accurate and stable variable frequency oscillator is programmable over a wide range of frequency by voltage, current, resistor or capacitor. In addition direct selection of one of four spot frequencies is facilitated by using the on-chip binary interface, which accepts standard logic levels at very low logic '1' input currents.

The differential input phase comparator has a wide common mode input voltage range. It has a high gain limiting amplifier at its input requiring only 1mV input to maintain lock range in a typical phase-locked loop. The current output is programmable from zero to over 2mA by an external resistor or current input, and the gain is voltage – current – or resistance – programmable from zero to greater than 10,000.

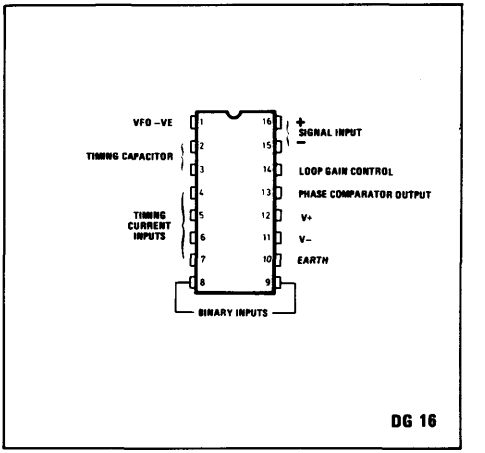


Fig. 1 Pin connections (top view)

FEATURES

- VFO Frequency Variable Over 100: 1 Range With Same Capacitor: Linearity 0.2%
- VFO Temperature Coefficient: 20 ppm/°C Typ.
- Supply sensitivity 20 ppm/% Typ.
- VFO Phase-Continuous at Transitions
- Binary Interface

QUICK REFERENCE DATA

Supply Voltages	±6V
Operating Temperature Range	0°C to +70°C
Supply Currents	1.5mA typ.

APPLICATIONS

- Modems
- Modulators
- Demodulators
- Tone Decoders
- Tracking Filters
- Waveform Generators
- Stable Current-Controlled Oscillators

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±7.5V
Storage temperature	–55° to +175°C
Operating temperature	–55° to +125°C
Input voltages	Not greater than supplies

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Supply voltage: ±6V
T_A: +25°C ±5°C

Characteristics	Pins	Value			Units	Conditions
		Min.	Typ.	Max.		
Variable frequency oscillator						
Initial frequency offset error		−3	±1	+3	%	
Normal mark/space ratio		0.98	1.00	1.02	–	
Temp. coefficient of frequency			±20		ppm/°C	See note 1
Frequency variation with supplies	11, 12		±20		ppm/%	
Voltage at timing current inputs	4, 5, 6, 7		±10		mV	See note 2
Max. freq. of oscillation			0.5		MHz	
Binary inputs						
V_{in} to guarantee logic 'low'	8, 9			+0.6	V	See note 3
V_{in} to guarantee logic 'high'	8, 9	+2.4			V	
Input current	8, 9		0.05	0.25	mA	V_{in} = +3.0V
Phase comparator						
Differential I/P offset voltage	15, 16		±2		mV	V_{out} = 0V
Input bias current	15, 16		0.05	2.5	μA	V_{in} = 0V
Differential input resistance	15, 16		100		kΩ	
Common mode I/P voltage range	15, 16	± 4			V	
Differential I/P to limit (AC)	15, 16		1.0	10	mV	See note 4
Output current	13, 14	±1.0	±2.0	±5.0	mA	I_{14} = 250μA
Current gain (pin 14 to pin 13)	13, 14	±4	±10		–	See note 5
Transconductance, O/P/diff.I/P	13, 15, 16	±100	±250		mA/V	See note 5
Output voltage, linear range	13	±5	±5.5		V	
Output current	13			±2	mA	I_{14} = 0

NOTES

1. With a timing current of 60μA and f = 1kHz (C = 0.01μF, R = 100kΩ, supply voltages = ±6V), the temperature coefficient of frequency of the SL652C is typically ±2.5ppm/°C over the range 0°C to +40°C.
2. This voltage applies for timing currents in the range 20μA to 2mA and with the relevant input selected. In the unselected state the voltage is typically +0.6V.
3. The 'low' state is maintained when the inputs are open-circuited.
4. Limiting will occur earlier if the output (pin. 13) voltage-limits first.
5. For a control current input to pin. 14 of 250μA. The sign of the transconductance is positive when the signal input is positive and the VFO output (or phase comparator input) is 'high'.

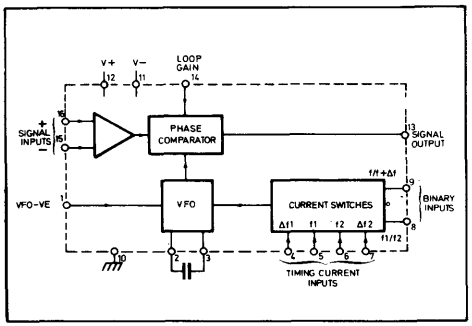


Fig. 2 SL652C block diagram

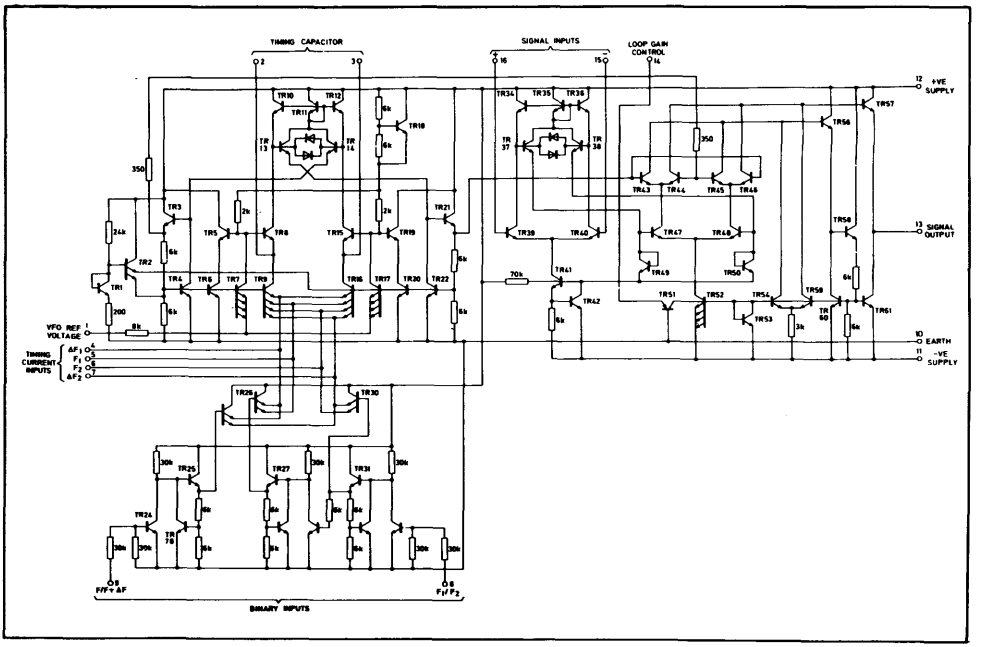


Fig. 3 Circuit diagram of SL652

OPERATING NOTES

Basic VFO Relationships

The oscillator output is normally taken from the phase comparator output by biasing the signal inputs a few hundred millivolts apart. If a direct oscillator output is required when the phase comparator is otherwise employed, it should be taken from pin 2 or 3 (which may affect oscillator stability). Alternatively, an SL651C can be used in place of the SL652C.

The VFO free-running frequency is inversely proportional to the value of the tuning capacitor C, connected to pins 2 and 3, and directly proportional to the VFO timing current (see Fig.4). Four current switches, controlled by TTL-compatible logic inputs on pins 8 and 9 select a combination of external resistors (connected to pins 4, 5, 6 and 7) which determine the VFO timing current. When both logic inputs are low, open-circuit, or connected to OV however, then only the current switch associated with pin 5 is closed. The VFO timing current is then determined solely by the value of one resistor (R2 in Fig. 4), and by the negative voltage connected to that resistor.

In this simplified configuration, as shown in Fig. 5 the VFO frequency is determined by the relationship.

$$f = \frac{1}{CR}\frac{V_R}{V_1}$$

where f is in kHz, V in volts, C in μF and R in kΩ.

If the timing resistor R is returned to the VFO negative supply (pin 1) then

$$V_R = V_1$$

$$\text{and } f = \frac{1}{CR}$$

Pin 1 is normally connected to the chip negative supply; if, however, pin 1 is connected to a separate negative supply then the VFO can be voltage-controlled, and the VFO frequency will be:

$$f = \frac{1}{CR}\frac{V-}{V_C}$$

where V– is the chip and timing resistor negative supply and V_C is the control voltage connected to pin 1.

The timing current should be between 20μA and 2mA, corresponding to a value for R between 3kΩ and 300kΩ with supplies of ±6V. For accurate timing, CR should be greater than 5μs.

When the binary interface is used as shown in Fig. 4, the VFO free-running frequency is dependent on the logic input states, as shown in Table 1.

Pin 8	Pin 9	Timing Pins	VFO Frequency
LO	LO	5	$\frac{1}{CR_2}$
LO	HI	4 & 5	$\frac{1}{CR_2}+\frac{1}{CR_1}$
HI	LO	6	$\frac{1}{CR_3}$
HI	HI	6 & 7	$\frac{1}{CR_3}+\frac{1}{CR_4}$

Table 1 Binary interface relationships

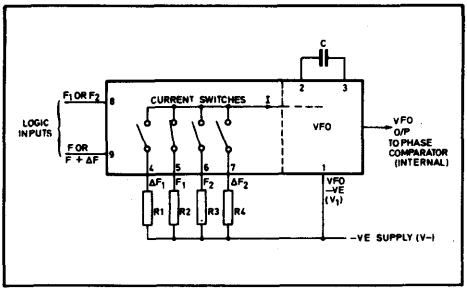


Fig. 4 VFO and binary interface

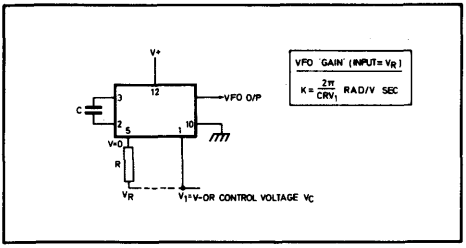


Fig. 5 VFO basic configuration

Phase Comparator

The phase comparator parameters are defined as follows (see Fig. 6):

$$\text{Overall transconductance} = \frac{I_{13}}{V_{16}-V_{15}}$$

$$\text{Overall voltage gain} = \frac{V_{13}}{V_{16}-V_{15}}$$

The input amplifier will limit when the peak input ($V_{16} - V_{15}$) exceeds ±5mV (typ.). It is recommended that R_L is kept below 5kΩ to avoid saturating the output and introducing de-saturation delays.

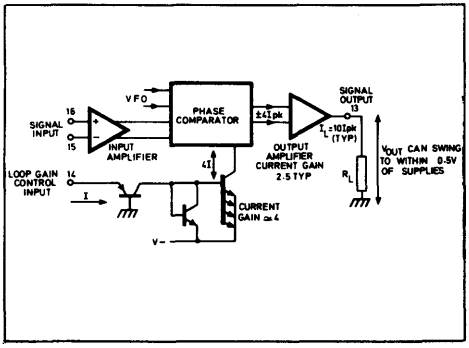


Fig 6. Phase comparator

PLESSEY
Semiconductors

SL1001A

MODULATOR/DEMODULATOR

The SL1001A is a bipolar monolithic integrated circuit double balanced modulator, designed primarily for use in telephone transmission equipment, but equally suitable for any application where the modulation function is required.

The device employs conventional 'tree' configuration multiplier circuits. Careful design of the circuit layout results in low carrier and signal leak levels, with high dynamic range and good linearity. Internal bias is provided, allowing direct balanced transformer input, or single-ended capacitor drive.

A two-stage common collector output structure is used to provide a low output impedance.

A pair of diodes is included to provide optional carrier input limiting.

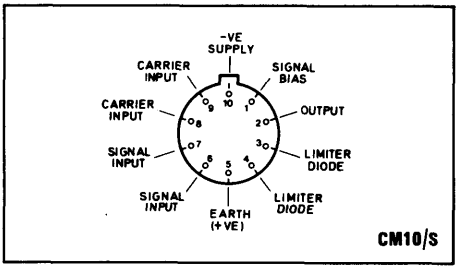


Fig.1 Pin connections (bottom)

FEATURES

- High Carrier and Signal Suppression: 50dB
- Unity Conversion Gain
- Low Noise Level: −112dBmp
- High Intermodulation Suppression: 58dB
- Low Supply Current: 6mA
- Diodes Included for Limiting

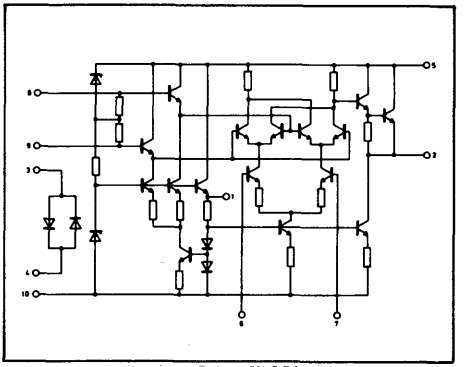


Fig.2 Circuit diagram

APPLICATIONS

- Telephone Transmission Equipment
- Suppressed Carrier and Amplitude Modulation
- Synchronous Detection
- FM Detection
- Phase Detection

QUICK REFERENCE DATA

Supply Voltage	−15V
Supply Current SL1001A	6mA
Carrier Level	125mVrms (Min.)
Signal Level	Up to 600mVrms
Output Current SL1001A	3.5mA peak (Typ.)
Temperature Range	−25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 22°C ± 2°C
Circuit ref: Figs.3 and 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Conversion gain	−1	0	+1	dB	
Signal input impedance		150		kΩ	Pins 6 & 7
Carrier input impedance	7	10	13	kΩ	Pins 8 & 9
	3.3	5	6.7	kΩ	Pins 8 & 5 or 9 & 5
Output impedance		12		Ω	Pin 2
Signal suppression	20	50		dB	Signal 170mV, Carrier 500mV
Carrier suppression	20	40		dB	
2nd harmonic suppression		40		dB	
Carrier compression			0.1	dB	For ± 3dB on 500mV
Supply line suppression		50		dB	Supply line resistance=500Ω
Sig. and carrier band width	200			kHz	
Carrier level	125			mVrms	
Signal level			600	mVrms	
Output current		3.5		mApk	
Noise level		−112	−105	dBmp	Weighted speech band
Intermod. products		−58		dB	Signals 2 X 170mV
Gain stability		0.12		dB	+5°C to +55°C
		0		dB	± 10% supply
Adjusted carrier suppression		70		dB	See Fig.5

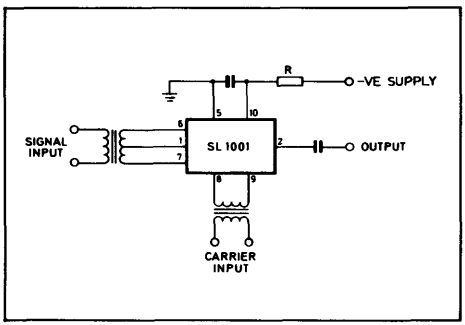


Fig.3 Transformer input

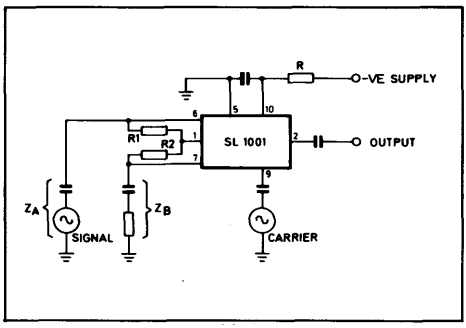


Fig.4 Unbalanced input

OPERATING NOTES

1. A resistance in series with the supply (Pin 10) is usually advisable, to improve the supply rejection and reduce the circuit voltage.
2. For good carrier suppression, the signal input bias resistors should be equal and have a value less than 5kΩ.
3. For improved intermodulation suppression, Pin 1 may be decoupled, preferably with a 100Ω resistor in series with Pin 1.

   If Pin 1 is not decoupled, noise is optimised when an unbalanced drive is used, by providing equal source impedances for Pins 6 and 7.
4. Low leakage input capacitors are advisable for the input connections to avoid inducing carrier or signal leakage.
5. Carrier suppression may be improved by using the circuit of Fig.5, and adjusting for minimum leakage.
6. This device is also available with tin-dipped leads, order as SL1001AM.

OPERATING CONDITIONS (see Figs.3 and 4)

Parameter	Value	Units	Condition
Supply voltage	−15	V	Pin 10
Supply current	6	mA	
Input bias current	5	μA	Pins 6 & 7
Dynamic resistance	8	kΩ	Pins 5 to 10
Output quiescent voltage	−3	V	Pins 2 to 5
Temperature range	−25 to +125	°C	

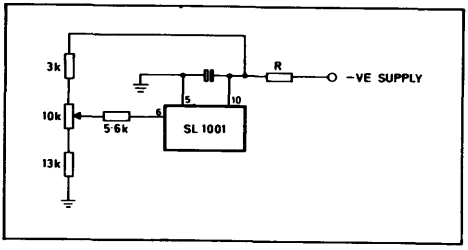


Fig.5 Carrier suppression adjustment

ABSOLUTE MAXIMUM RATINGS

Supply voltage (via 820Ω)	−30V
Storage temp. range	−55°C to + 175°C
Free air operating temp. range	−40°C to + 150°C

PLESSEY
Semiconductors

SL1021 A & B

TELEPHONE CHANNEL AMPLIFIER

The SL1021 A and B are bipolar monolithic integrated circuit amplifiers designed for use as channel amplifiers in telephone transmission equipment and satisfy the requirements of the British Post Office channel translating apparatus (RC5467).

The two variants A and B are distinguished by guaranteed output levels of +10dBm and +13dBm, respectively, other parameters being identical.

The main feature of these devices is the provision of a temperature-stable DC operated remote gain control facility having an adjustable range of control.

The connections provided allow a variety of uses, including fixed gain amplification with various feedback configurations.

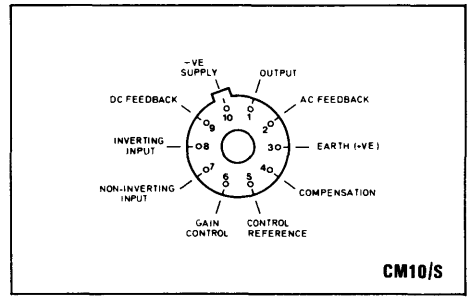


Fig. 1 Pin connections

FEATURES

- Up to +13dBm O/P into 600Ω (Class A)
- Temperature insensitive remote DC gain control
- Non-interactive adjustment of:
  - Gain
  - Gain Range
  - Output Return Loss
- 1:1 600Ω Transformer output can be optimized for low inductance using 2-element filter configuration
- Power Bandwidth: 150kHz (fixed gain, Fig. 4)
- Small Signal gain Bandwidth: 3MHz (see Fig. 4)

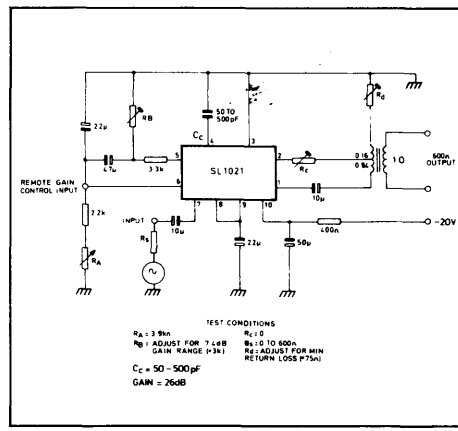


Fig. 2 SL1021 test circuit and typical application

APPLICATIONS

- Telephone Communications
- Channel Group Translation Equipment
- Radio – communications
- Small Signal Processing

QUICK REFERENCE DATA

Supply Voltage	−20V (via 400Ω)
Supply Current	9mA
Gain Control Current	0.5mA
Temperature Range	−25°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} 22°C ± 2°C

These characteristics are those obtained using the test circuit of Fig. 2, the gain range and output impedance being adjusted as indicated.

Characteristics	Value			Units	Conditions
	Min.	Typ,	Max.		
Gain (reference gain G)	24.5	26	27.5	dB	
Gain/R_S			28	dB	R_S = 600Ω to 3kΩ
Gain range		7.4		dB	Adjusted
Gain law					
R_A = 125Ω	3.9	4.1	4.3	dB	Relative to G
R_A = 9kΩ	−3.5	−3.3	−3.1	dB	
Gain/temperature	−0.1		+0.1	dB	Relative to G, T = 10°C to 45°C
Gain/V_S			0.1	dB	V_S = −20V ± 1V
Distortion					
2nd harmonic			−36	dBm0	At 10dBm output
3rd harmonic			−45	dBm0	
Overload					
SL1021A	10	13		dBm	Class A operation
SL1021B	13	15		dBm	
Noise			−76	dBmP	Proportional to G
Output impedance		600		Ω	Adjusted
Return loss	20			dB	250Hz to 3.4kHz
Input impedance	10			kΩ	Variable with R_A and R_S
Gain at reduced V_S	25.5			dB	V_S = −17.5V See Fig.2
Overload at reduced V_S	7			dBm	V_S = −17.5V
Gain control interaction between channels (change in gain for 3.3 mA current change)			0.25	dB	Equivalent to 11 channels, Common R_A earth return
Frequency response	240		3400	Hz	±0.05dB ref. 800Hz
Bandwidth			100	kHz	C_C = 50pF

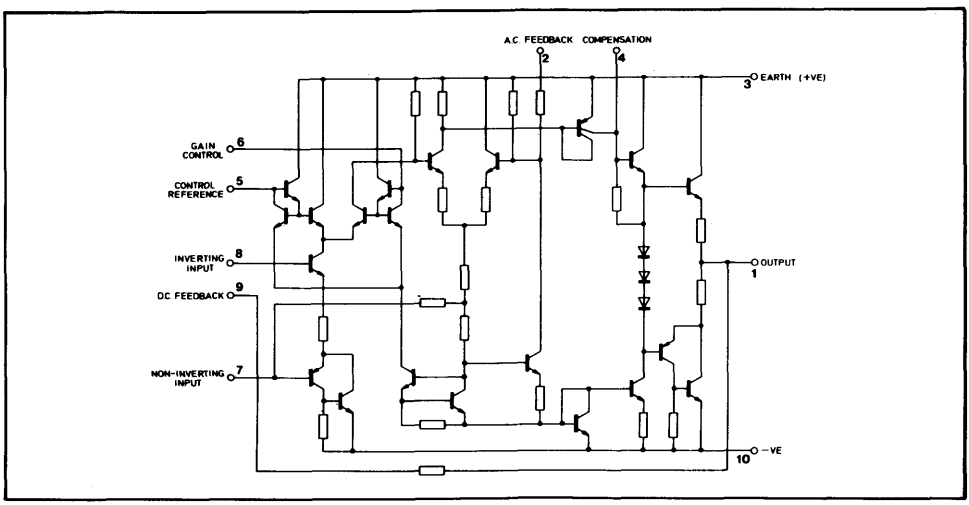


Fig. 3 SL1021 equivalent circuit

OPERATING CONDITIONS (see Fig. 2)

Parameter	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11.0	mA	$R_A = 0$
		7.0		mA	$R_A = 11k\Omega$
Supply voltage		−20		V	Via 400Ω
Supply voltage on chip		−17		V	Pin 10
Supply maximum			−23	V	Pin 10
Control current		0.5		mA	$R_A = 0$
		0.26		mA	$R_A = 10k\Omega$
Control current change			0.3	mA	R_A = 0 to 11kΩ
Operational temp.	−25		+125	°C	
Fixed gain application (see Fig. 4)					
Optimum load		100		Ω	
Power output		20		mW	Class AB
Power bandwidth		150		kHz	10mW
Gain		20		dB	Values as Fig. 4
Frequency response		3		MHz	Small signal

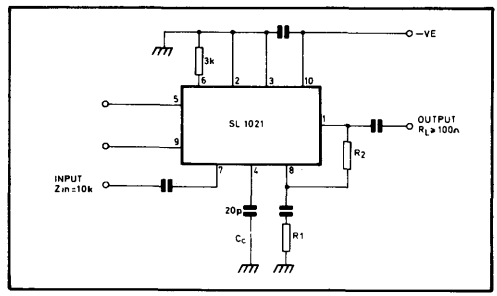


Fig. 4 Fixed gain amplifier, Class A or AB

OPERATING NOTES

1. The control decoupling capacitors should be of a low leakage type.
2. Other values of control resistors are possible if other gains/gain ranges are required. However, the parallel resistance to earth from pins 5 and 6 should be ⩽8kΩ at all settings.
3. If the control resistance is increased or open circuited, the amplifier gain will decrease to zero. (See Fig. 4 for fixed gain use).
4. The compensation capacitor can be increased to reduce the frequency response and power bandwidth.
5. The gain may be increased from the value of Fig. 2 (26dB nominal) by increasing R_c, the gain increase being given by:

$$\frac{R_c + 8.5}{8.5} \pm 20\%$$

where R_c is in kΩ.

Because of temperature coefficient mismatch between R_C and internal resistors, the gain stability may be degraded with temperature.

6. The case is connected to pin 10 (−ve supply). To avoid damage to the device when operating with a positive earth system, care should be taken to prevent the case from becoming earthed.
7. This device is also available with tin-dipped leads, order as SL1021AM.

ABSOLUTE MAXIMUM RATINGS

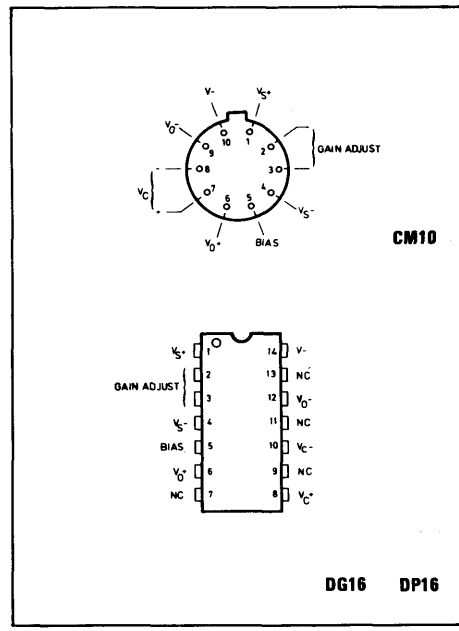
Supply voltage (via 400Ω)	−30V
Storage temp. range	−55°C to +175°C
Free air operating temp. range	−40°C to +130°C

PLESSEY
Semiconductors

SL1496C SL1596C

DOUBLE-BALANCED MODULATOR/DEMODULATOR

The SL1596C and SL1496C are versatile monolithic integrated circuit double balanced modulators/demodulators, designed for use where the output voltage is the product of the signal input voltage and the switching carrier voltage. The SL1596 has an operating temperature range of −55°C to +125°C, whilst that of the SL1496 is 0°C to +70°C.



FEATURES

- Carrier Suppression — 65dB Typ. @ 500 kHz, 50dB Typ. @ 10 MHz
- Common Mode Rejection — 85dB Typ.
- Gain and Signal Handling Both Adjustable
- Balanced Inputs and Outputs

APPLICATIONS

- DSB, DSBSC, AM Modulation
- Synchronous Detection
- FM Detection
- Phase Detection
- Telephone FDM Systems

ORDERING CODES

SL1496C — CM, SL1496C — DG, SL1496C — DP
SL1596C — CM, SL1596C — DG

ABSOLUTE MAXIMUM RATINGS

(Pin number reference to CM package)

Applied voltage* 30V
Differential input signal (V_7—V_8) ±5V
Differential input signal (V_4—V_1) ± (5+1$5R_E$)V
Bias current (I_5) 10mA
Operating temperature range
SL1496 0 °C to +70 °C
SL1596 −55 °C to +125 °C

CM Package

Storage temperature range	−55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	680mW

DG Package

Storage temperature range	−55 °C to +175 °C
Junction temperature	+175 °C
Package dissipation (25 °C)	600mW

DP Package

Storage temperature range	−55 °C to +125 °C
Junction temperature	+125 °C
Package dissipation (25 °C)	500mW

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):–
$V^+ = +12V$ DC, $V^- = -8V$ DC, $I_5 = 1.0$ mA DC, $R_L = 3.9\ k\Omega$, $R_e = 1.0\ k\Omega$ $T_A = +25°C$
All input and output characteristics single-ended, unless otherwise stated.

Characteristic*	SL1596 Min	SL1596 Typ	SL1596 Max	SL1496 Min	SL1496 Typ	SL1496 Max	Units
Carrier Feedthrough							μV(rms)
V_C = 60 mV(rms) sinewave and offset adjusted to zero f_C = 1.0 kHz	–	40	–	–	40		
f_C = 10 MHz	–	140	–	–	140	–	
V_C = 300 mVp-p square wave							mV(rms)
offset adjusted to zero f_C = 1.0 kHz	–	0.04	0.2	–	0.04	0.4	
offset not adjusted f_C = 1.0 kHz	–	20	100	–	20	200	
Carrier Suppression							dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sinewave	50	65 •	–	40	65	–	
f_C = 10 MHz, 60 mV(rms) sinewave	–	50	–	–	50	–	
Signal Gain V_S = 100 mV(rms), f = 1.0 kHz; $\lvert V_C \rvert$ = 0.5 V DC	2.5	3.5	–	2.5	3.5	–	V/V
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							
Parallel Input Resistance	–	200	–	–	200	–	kΩ
Parallel Input Capacitance	–	2.0	–	–	2.0	–	pF
Single-Ended Output Impedance, f = 10 MHz							
Parallel Output Resistance	–	40	–	–	40	–	kΩ
Parallel Output Capacitance		5.0	–	–	5.0	–	pF
Input Bias Current $\frac{I_1 + I_4}{2}$; $\frac{I_7 + I_8}{2}$		12	25	–	12	30	μA
Input Offset Current $(I_1 - I_4)$, $(I_7 - I_8)$		0.7	5.0	–	0.7	7.0	μA
Average Temperature Coefficient of Input Offset Current (T_A = −55°C to +125°C)	–	2.0	–	–	2.0	–	nA/°C
Output Offset Current $(I_6 - I_9)$	–	14	50	–	14	80	μA
Average Temperature Coefficient of Output Offset Current (T_A = −55°C to +125°C)	–	90	–	–	90	–	nA/°C
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz	–	5.0	–	–	5.0	–	Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz, $\lvert V_C \rvert$ = 0.5 V DC	–	- 85	–	–	–85	–	dB
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)	–	8.0	–	–	8.0	–	V DC
Differential Output Voltage Swing Capability	–	8.0	–	–	8.0	–	Vp-p
Power Supply Current							mA DC
$I_6 + I_9$	–	2.0	3.0	–	2.0	4.0	
I_{10}	–	3.0	4.0	–	3.0	5.0	
DC Power Dissipation	–	33	–	–	33	–	mW

*Pin numbers are given for TO-5 package.

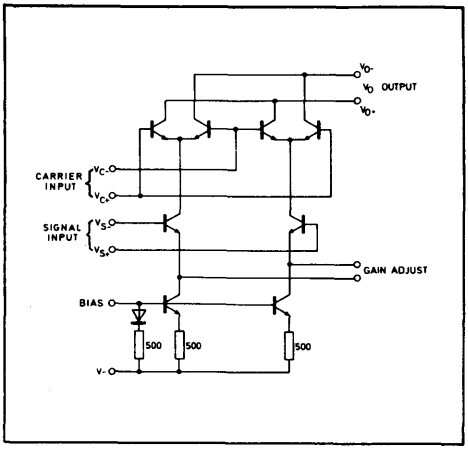


Fig. 2 Circuit diagram

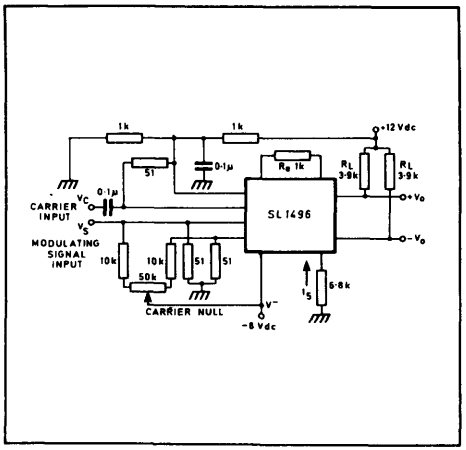


Fig. 3 Typical modulator circuit

PLESSEY
Semiconductors

PRELIMINARY INFORMATION

SL8204

TELEPHONE TONE RINGER

The SL8204 is a telephone set tone ringer IC. It is packaged in an 8 pin DIL Minidip. The unit is designed for use as a telephone set bell replacement, or as an extension ringer. The SL8204 will drive a speaker in place of the existing bell, using power supplied from the telephone line.

Two audio oscillators are incorporated. The low frequency oscillator shifts the high frequency oscillator between 508 and 635Hz at a 10Hz rate. These frequencies are determined by external components which may be changed as desired. The IC has a built-in threshold circuit with hysteresis which prevents false triggering, eliminates rotary dial 'chirps', and provides positive switching operation.

The IC may also be used for other applications requiring an attention-getting sound. Output power from the built-in amplifier is nominally 35mW, and will produce a maximum 90dBA sound pressure-level from a properly baffled 2 inch speaker.

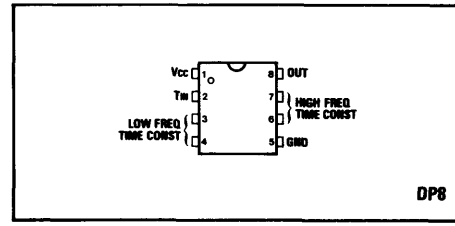


Fig.1 Pin connections - top view

FEATURES

- Low Current Drain
- Small Size (mini-DIP)
- Adjustable Frequency
- Threshold Circuit Prevents False Triggering and Rotary Dial 'Chirps'
- Built-In Hysteresis For Positive Enable
- Few External Components
- Up To 90dBA Sound Pressure Level

ABSOLUTE MAXIMUM RATINGS

Supply voltage	30V d.c.
Storage temperature range	-65°C to +150°C
Operating temperature range	-45°C to +65°C

APPLICATIONS

- Telephone Bell Replacement
- Extension Ringers

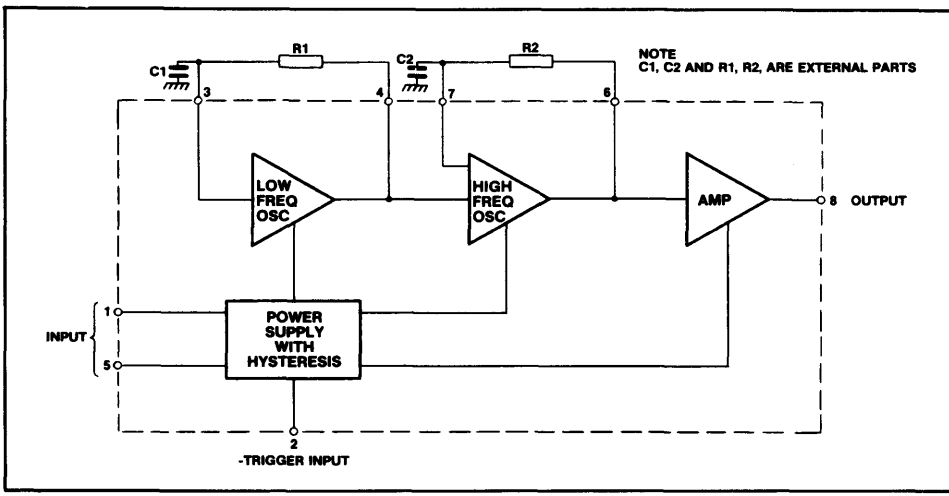


Fig.2 SL8204 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = -45°C to +65°C

Characteristic	Value			Units	Conditions		
	Min.	Typ.	Max.				
Initiation supply voltage V_{SI}	17	19	21	V	See Fig.4		
Sustaining voltage V_{SUS}	9.7	11.5	13	V	See Fig.4		
Supply current I_{SI}	1.4	2.5	4.2	mA	No load. See Fig.4		
Supply current I_{SUS}	0.7	1.4	2.5	mA	See Fig.4		
K1, f_{H1} (constant) See Eq.1	1/1.681	1/1.515	1/1.380				
f_{H1} (frequency)	458	508	558	Hz	R_2 = 191k	C_2 = 6800pF	
K2, f_{H2} (constant) See Eq. 2	1.190	1.250	1.310				
f_{H2} (frequency)	545	635	731	Hz	R_2 = 191k	C_2 = 6800pF	
K3, f_L (constant) See Eq. 3	1/1.367	1/1.234	1/1.118				
f_L (frequency)	9	10	11	Hz	R_1 = 173k	C_1 = 0.47μF	
Operating voltage	-	-	29	V			
Output voltage high	18.0	19.0	20.0	V	V_{CC} = 21V Pin 6 = 6V	I(Pin 8) = -15mA Pin 7 = GND	
Output voltage low	0.5	0.9	1.3	V	V_{CC} = 21V Pin 6 = GND	I(Pin 8) = 15mA Pin 7 = 6V	
Trigger voltage V_T	8.5	9.5	10.5	V	V_{CC} = 15V See Note 1		
Trigger current I_T		20.0	1000	μA	See Notes 1 and 3		
Disable voltage V_D		0.4	0.8	V	T_{amb} = 25°C See Note 2		
Disable current	-40	-50		μA	T_{amb} = 25°C See Note 2		
I_{IN} (Pin 3)	-	-	500	nA	Pin 3 = 6V	Pin 4 = GND	
I_{IN} (Pin 7)	-	-	500	nA	Pin 7 = 6V	Pin 6 = GND	
I (Pin 4) Source V_{CC} = V_{SUS}	150	300	600	μA	Pin 3 = GND	Pin 4 = GND	
I (Pin 4) Sink V_{CC} = V_{SUS}	100	200	350	μA	Pin 3 = 6V	Pin 4 = 5V	
I (Pin 6) Source V_{CC} = V_{SUS}	80	175	350	μA	Pin 6 = GND	Pin 7 = GND	Pin 4 = GND
I (Pin 6) Source V_{CC} = V_{SUS}	125	250	500	μA	Pin 6 = GND	Pin 7 = GND	Pin 4 = 8V
I (Pin 6) Sink V_{CC} = V_{SUS}	70	125	250	μA	Pin 6 = 5V	Pin 7 = 6V	Pin 4 = GND
I (Pin 6) Sink V_{CC} = V_{SUS}	100	200	300	μA	Pin 6 = 5V	Pin 7 = 6V	Pin 4 = 8V

NOTES
1. V_T and I_T are the conditions applied to Pin 2 to start oscillation for $V_{SUS} < V_{CC} < V_{SI}$
2. V_D and I_D are the conditions applied to Pin 2 to inhibit oscillation for $V_{SI} < V_{CC}$
3. Trigger Current must be limited externally

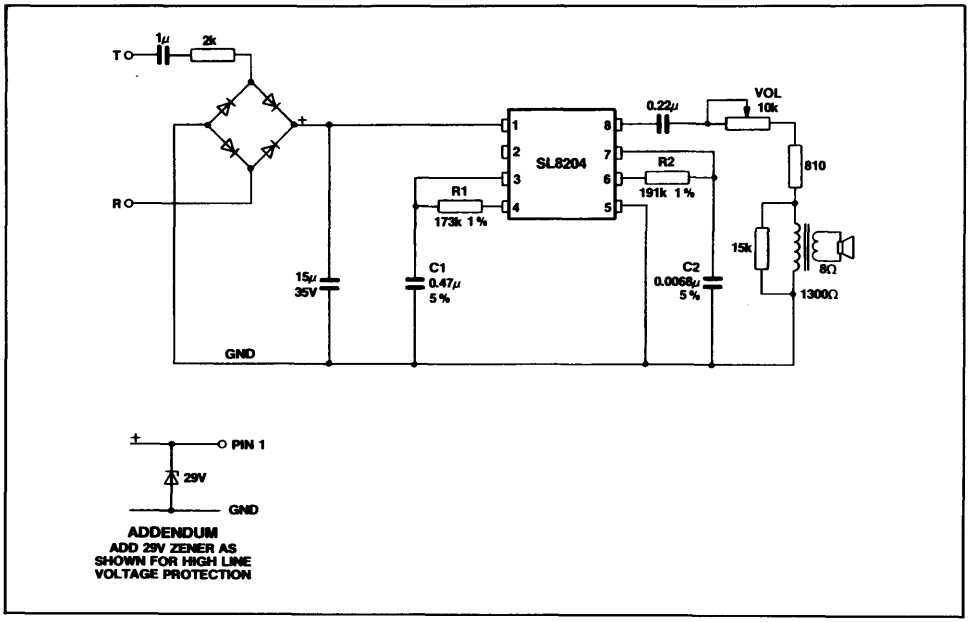


Fig.3 Circuit diagram - tone ringer

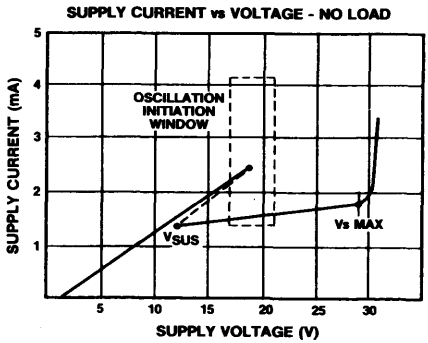


Fig.4 Tone ringer characteristics

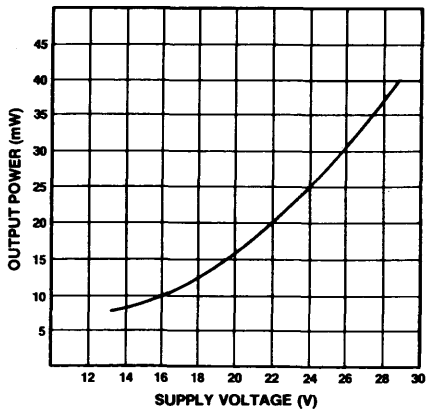


Fig.6 Typical power output

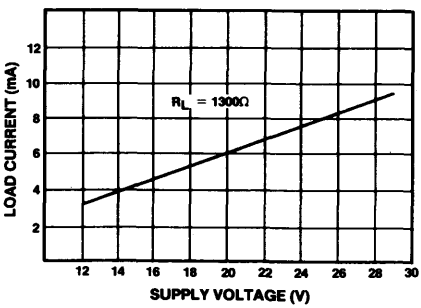


Fig.5 Typical RMS current

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SP1404BW, D3702

HIGH VOLTAGE INTERFACE CIRCUIT

The SP1404 is a bipolar integrated circuit comprising five individual digital current amplifier circuits. Each circuit accepts a logic input from TTL, CMOS or a similar source and drives a high-current load at the output. The outputs are capable of withstanding high negative voltages in the 'off' state, making the SP1404 particularly suited to telecommunications applications.

The D3702 is a version of the SP1404BW in 14 pin plastic package approved to BT specification.

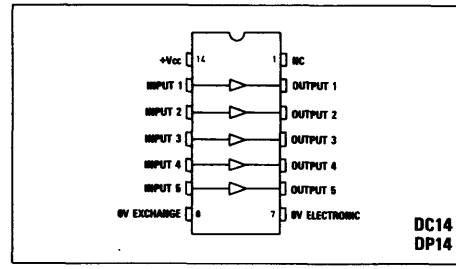


Fig. 1 Pin connections (viewed from underside)

CIRCUIT DESCRIPTION (FIG.2)

The SP1404 operates as a power amplifier interfacing from a voltage-level sensitive input to a high-current output switch. The input threshold is TTL-compatible, with a low input current requirement enabling one standard TTL output to drive many interfaces. The low input current requirement also makes it possible to use series current-limiting resistors to protect the SP1404 inputs.

Each element of the device performs an inverting function, i.e. a low voltage level on the input causes a high current in the output. If the input is left open-circuit, the output will be off and the output current will be zero.

The isolation of the integrated circuit is biased to the more negative of the two earth points by diodes D1 and D2 so that differences of up to (Vcc - 1) volts can be tolerated between the 'noisy' exchange earth and the 'quiet' electronic earth.

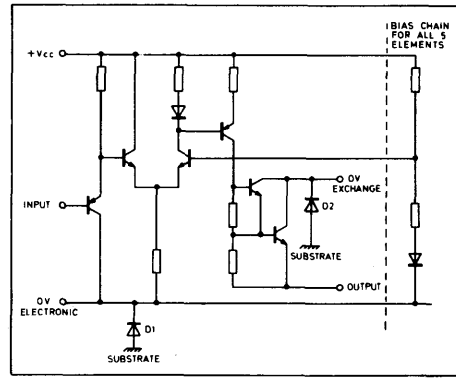


Fig. 2 Circuit diagram of one element

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated)
Temperature range = 0°C to +70°C
V_{CC} = +5V ± 0.5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input current		−20		μA	V_{in} = 0V
		−2		μA	V_{in} = V_{cc}
Output voltage			1.5	V	V_{in} = 0.8V, I_{out} = 50mA
Output current (Off state)			100	μA	V_{in} = 2V, V_{out} = -60V
Output current (On state)	50	80		mA	Vin = 0.8V
V_{CC} supply current		30		mA	V_{cc} = 5V, all inputs low
Total power dissipation		450		mW	V_{cc} = 5V, all inputs low all outputs I_{out} = 50mA

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +175°C
Chip operating temperature	+150°C
Ambient temperature (I_{out} = 50mA)	+85°C
Load current	80mA
Voltage between output and 'noisy' earth	−65V
V_{CC} to output voltage	75V
V_{CC} to electronic earth	7V
Input voltage	V_{CC} + 1V

PLESSEY
Semiconductors

SP1450B(B) & SP1455B(B)

PCM SIGNAL MONITOR CIRCUITS

The SP1450 and SP1455 are bipolar integrated circuits designed to monitor errors in three-level digital signals modulated by a three-alphabet 4B3T code such as MS43. They can also indicate the failure of positive or negative pulses in the signal. The high frequency capability allows operation in PCM systems up to 34M bit/s (SP1450) and 140M bit/s (SP1455). Facilities are provided to adjust input thresholds independently on each polarity of input and the error output can be interfaced with low speed CMOS circuitry or high speed ECL.

The SP1450B(B) and SP1455B(B) are similar to the SP1450B and SP1455B but are screened to MIL-STD-883, Method 5004, Class B.

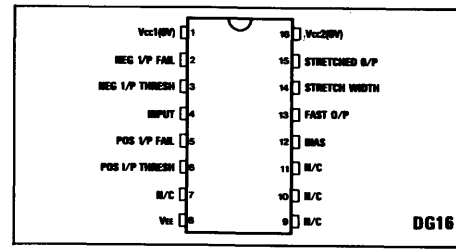


Fig.1 Pin connections (top view)

FEATURES

- *Suitable for 34, 120 and 140M bit/s PCM*
- Positive and Negative Input Signal Fail Outputs
- High Speed Error Output
- Low Speed 'Stretched' Output
- Low Power Consumption

APPLICATIONS

- PCM Telephone Transmission Terminal Equipment
- PCM Repeaters
- Error Checking Test Equipment

QUICK REFERENCE DATA

- Supply Voltage -4.4V to -5.25V
- Operating Temperature -10°C to +70°C
- Power Consumption 100mW typ
- Input Voltage Range ±450mV to ±1100mV (SP1450)
  ±450mV to ±600mV (SP1455)
- Thermal Resistance θj-a 100°C/W

ABSOLUTE MAXIMUM RATINGS

Supply voltage -8V
Reverse input current (pin 4) 5mA (continuous) 20mA (10us max)
Forward input current (pin 4) 20mA (10us max)
Storage temperature -55°C to +150°C
Operating temperature -10°C to +70°C
Junction temperature 150°C

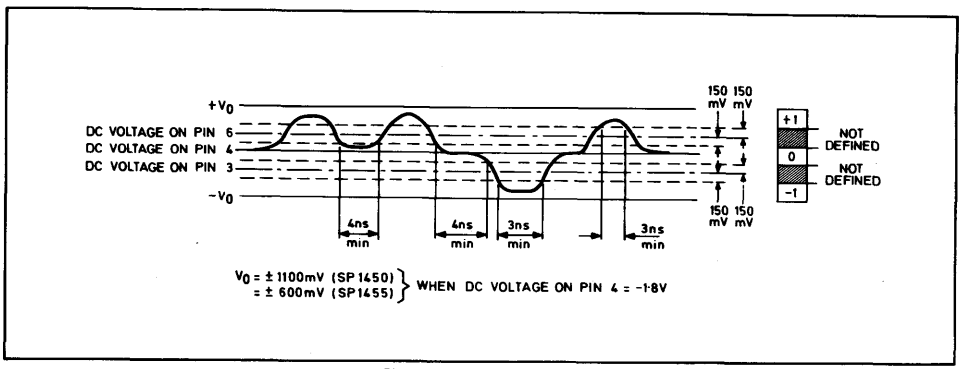


Fig.2 Input pulse wave form

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = Pins 1-16 = 0V
V_{EE} = Pin 8 = -5.0V
T_{amb} = +25°C
Input voltage range (pins 3,4,6) = -0.9V to -3.1V

DC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Output low, current	2	0.9	1.2	1.9	mA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2.0V
Output low, current	2	0.7	—	—	mA	Pin 2 = OV Pin 3 = —1.95V Pin 4 = —2.0V
Output high, current	2	—	—	1	µA	Pin 2 = OV Pin 3 = —2.3V Pin 4 = —2.0V
Output high, current	2	—	—	0.4	mA	Pin 2 = OV Pin 3 = —2.05V Pin 4 = —2.0V
Output low, current	5	0.9	1.2	1.9	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.3V
Output low, current	5	0.7	—	—	mA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —2.05V
Output high, current	5	—	—	1	µA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.7V
Output high, current	5	—	—	0.4	mA	Pin 5 = OV Pin 4 = —2.0V Pin 6 = —1.95V
Output low, current	13	6.0	7.0	9.0	mA	Pin 13,15 = OV Pin 3 = —1.7V Pin 4 = —2.0V Pin 6 = —2.3V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V Six pos. or neg. pulses on pin 4
Output high, current	15	—	—	1	µA	
Output high, current	13	—	—	1	µA	Pin 13, 15 = OV Pin 3 = —2.3V Pin 4 = —2.0V Pin 6 = —1.7V Pins 2,5 = OV 470 Ω pin 12 to —5V 27 kΩ pin 14 to —5V
Output low, current	15	0.5	0.75	—	mA	
Current consumption	1,16	—	20	25	mA	(Pins 2,5,13,15 = OV (Pins 3,6 = —2.3V (Pin 4 = —2.0V (27 kΩ resistor between (Pin 14 and —5V (Pin 12 open
Input bias current	3	—	—	40	µA	Pin 2 = OV Pin 3 = —1.7V Pin 4 = —2V
Input bias current	6	—	—	40	µA	Pin 4 = —2.0V Pin 5 = OV Pin 6 = —1.7V
Input bias current	4	—	—	80	µA	Pins 2,5 = OV Pins 3,6 = —2.3V Pin 4 = —2.0V

AC CHARACTERISTICS

Circuit reference: Fig.3
Input signal: Fig.2
T_{amb} = -10°C to +70°C
V_{EE} = -4.4V to -5.25V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Max. Input Frequency						
SP1450	13		—	25.5	M band/s	See note 1 below
SP1455	13		—	105	M band/s	
Stretched output pulse width	15	0.5	0.7	2	µS	$c_1 = 390$ pF $R_1 = 27$ kΩ using circuit of Fig. 7 (see note 2 below)
Error pulse width SP1455	13	4.25	—	5.25	nS	Input freq. 105 M band/s
Error pulse amplitude	13	300	—	—	mV	At max input frequency
Spurious pulse amplitude	13	—	—	50	mV	At max. input frequency

NOTE 1: These figures are the max.input symbol rates. For 4B3T codes, the effective bit rate is 4/3 x (input frequency).
NOTE 2: Resistor and capacitor values quoted are absolute values; temperature coefficients and tolerances have not been taken into account.

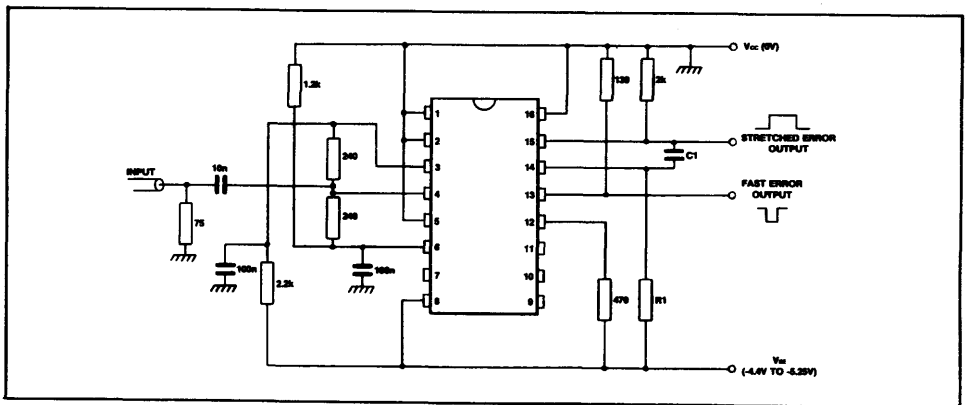


Fig.3 Functional test circuit

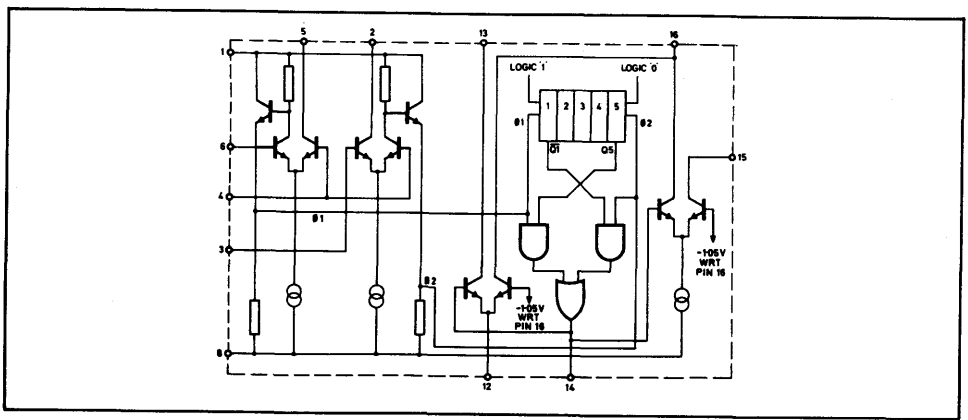


Fig.4 Circuit diagram of SP1450/SP1455

APPLICATIONS

The circuit shown in Fig.3 is designed to accept a three level (ternary) input signal as shown in Fig.2. The input is applied to pin 4 whilst fixed bias levels are maintained on pins 3 and 6. When a positive input pulse is applied at a level more positive than the bias on pin 6 the positive comparator output o 1 goes from '0' (V_{EE}) to '1' (V_{CC}). The 1-0 edge of this pulse clocks the five bit shift register one place to the right. Repeated operation will cause a pattern of logic '1's to be propagated along the shift register. When bit 5 is at logic '1' and the input is also positive an 'error' will occur at pins 13 and 15.

A negative input pulse at a level more negative than the voltage on bias pin 3 causes the negative comparator output o 2 to clock the shift register one place to the left. Repeated operation causes a pattern of logic '0's to be propagated along the shift register. When bit 1 is at logic '0' and the input is also negative an 'error' output will again occur at pins 13 and 15.

During normal operation the shift register can assume one of only six possible states as shown in Fig.5.

State	1	2	3	4	5
A	0	0	0	0	0
B	1	0	0	0	0
C	1	1	0	0	0
D	1	1	1	0	0
E	1	1	1	1	0
F	1	1	1	1	1

Fig.5 Shift register states

When power is initially connected other states may occur.

Two 'error' outputs are available. The fast output at pin 13 is negative going; the peak current is defined by a resistor connected between pin 12 and V_{EE} according to the formula:

$$I = \frac{3.3}{R} \text{ (e.g. 820 ohms; 4mA)}$$

A pullup resistor must then be connected between pin 13 and V_{CC} to give a suitable voltage swing. A suitable ECL interface is shown in Fig.6.

If, as in a repeater application, a fast output is not required, pin 12 should be left open and pin 13 connected to V_{CC} (pin 16).

A stretched output is available from pin 15 by connection of a capacitor between pins 14 and 15. A suitable circuit is shown in Fig.7.

Facilities are available at pins 2 and 5 to detect the absence of negative and positive going input signals. If these are not required pins 2 and 5 should be connected to V_{CC} (pin 1). A CMOS interface circuit is shown in Fig.8.

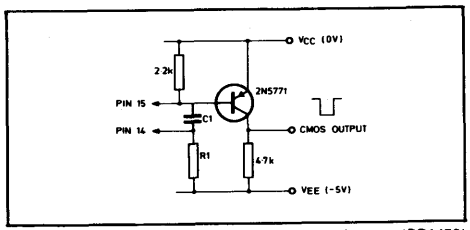


Fig.7(a) Interfacing with CMOS at the stretched output (SP1450)

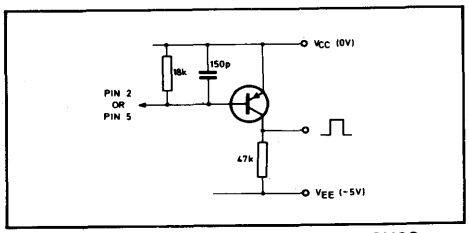


Fig.8 Interfacing with pulse fail output with CMOS

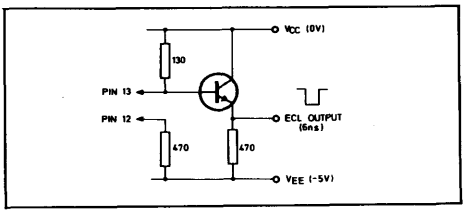


Fig.6 Interfacing with ECL at the output

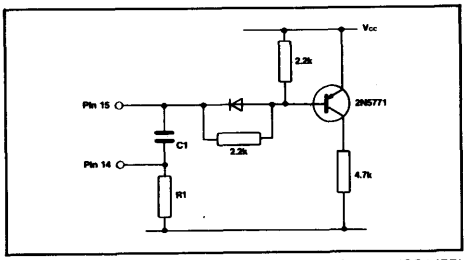
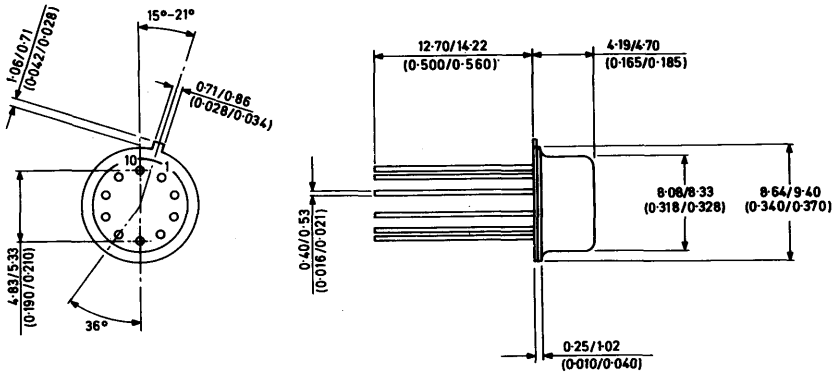
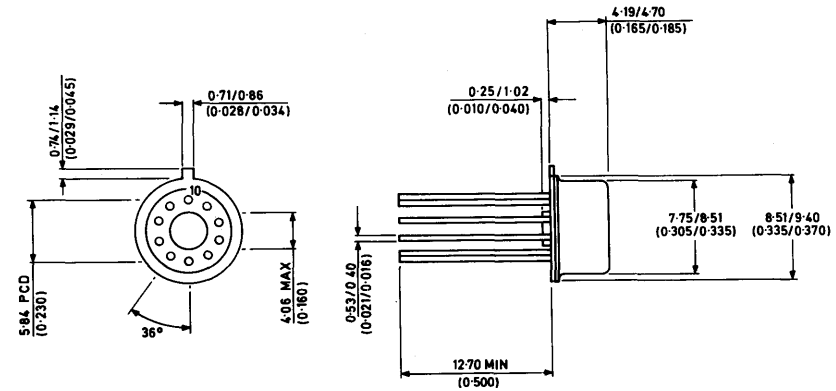


Fig.7(b) Interfacing with CMOS at the stretched output (SP1455)

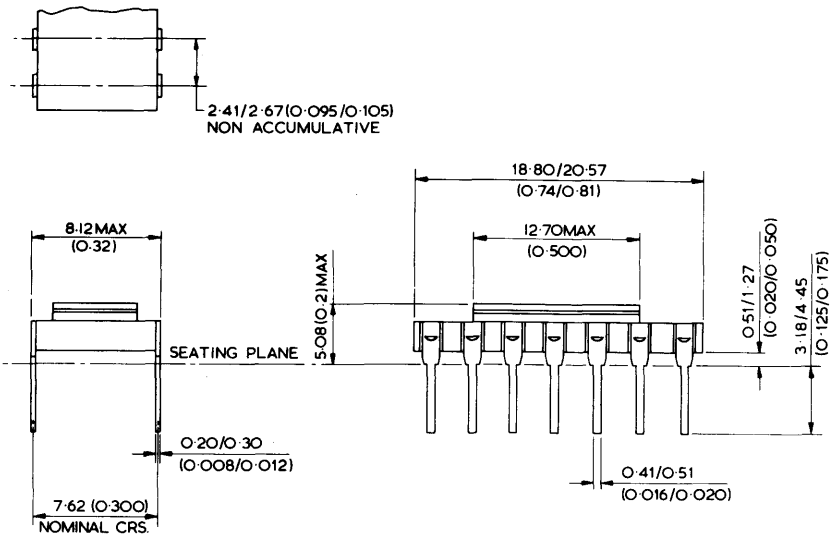
Package Outlines



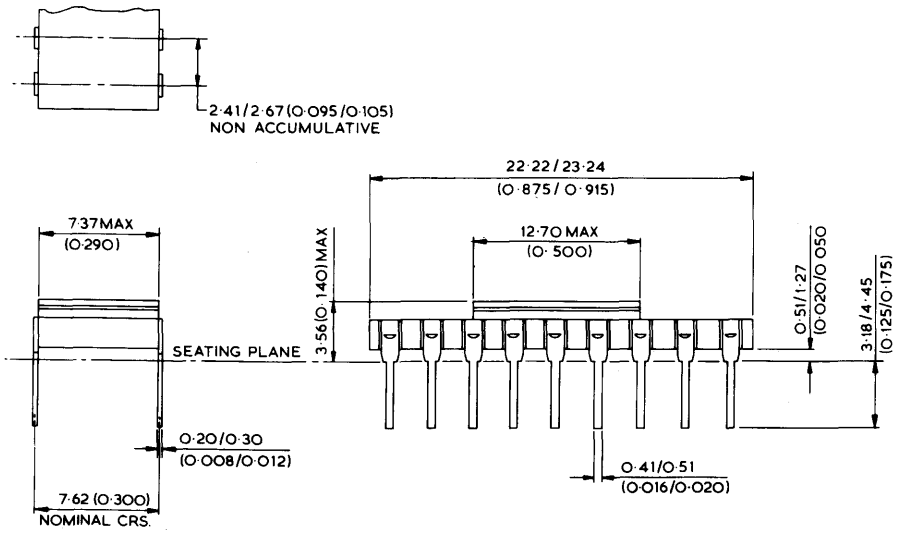
10 LEAD TO-5 **CM10**



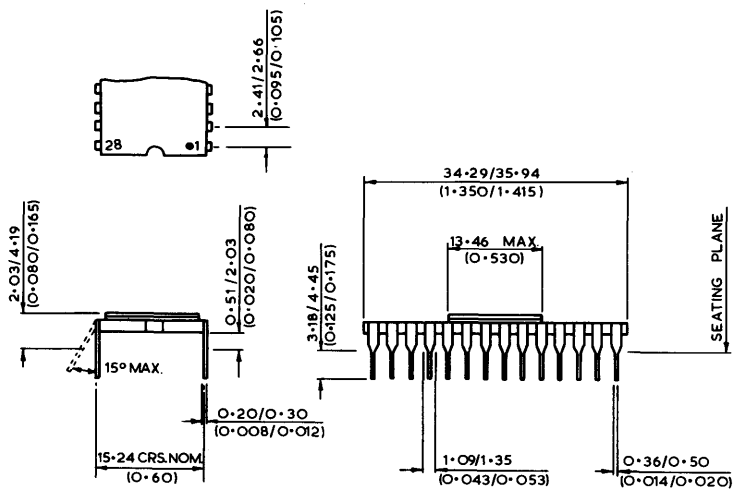
10 LEAD TO-100 (5.84mm PCD) WITH STANDOFF **CM10/S**



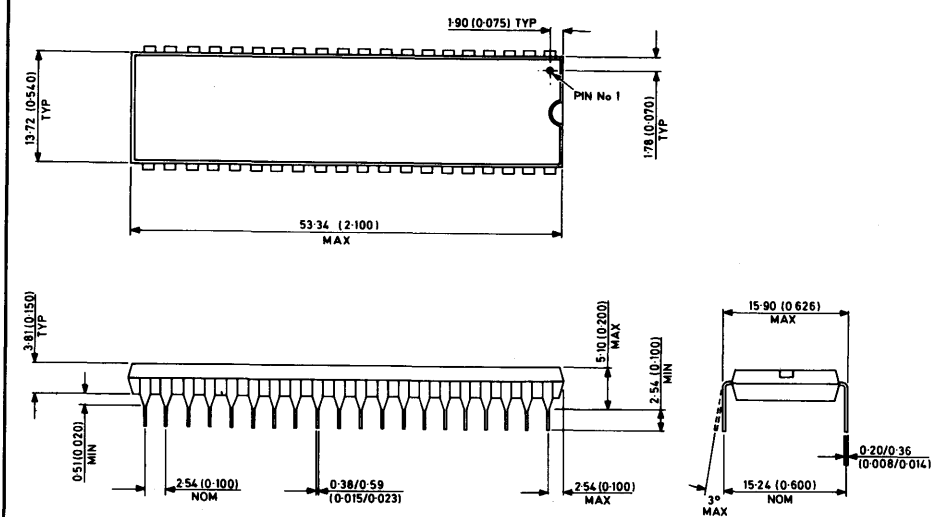
14 LEAD DILMON **DC14**



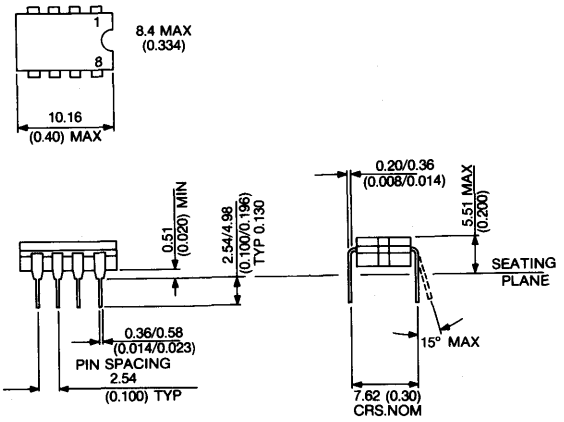
18 LEAD DILMON **DC18**



28 LEAD DILMON' **DC28**

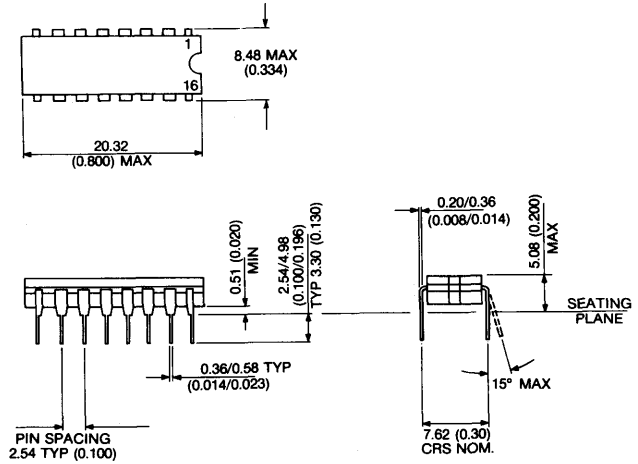


40 LEAD (SIDE BRAZED) DIL **DC40**



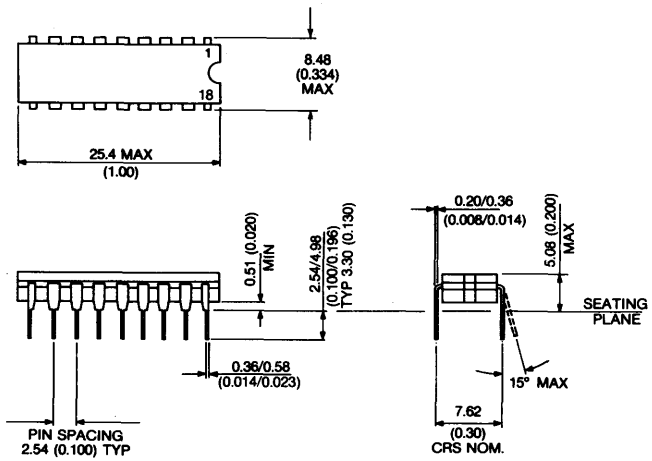
8 LEAD CERAMIC DIL
CERDIP - DG8

DG8



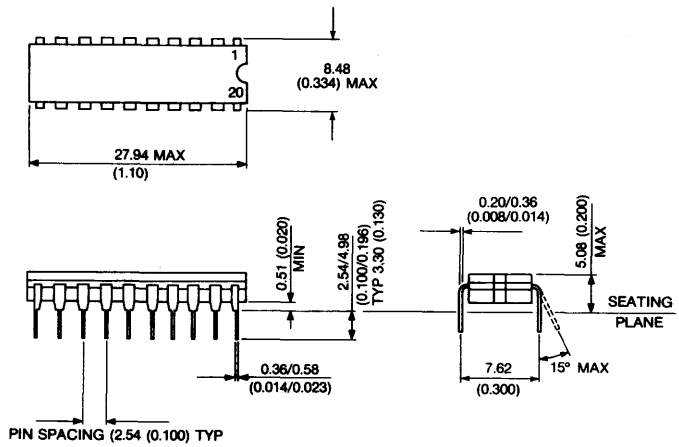
16 LEAD CERAMIC DIL
CERDIP - DG16

DG16



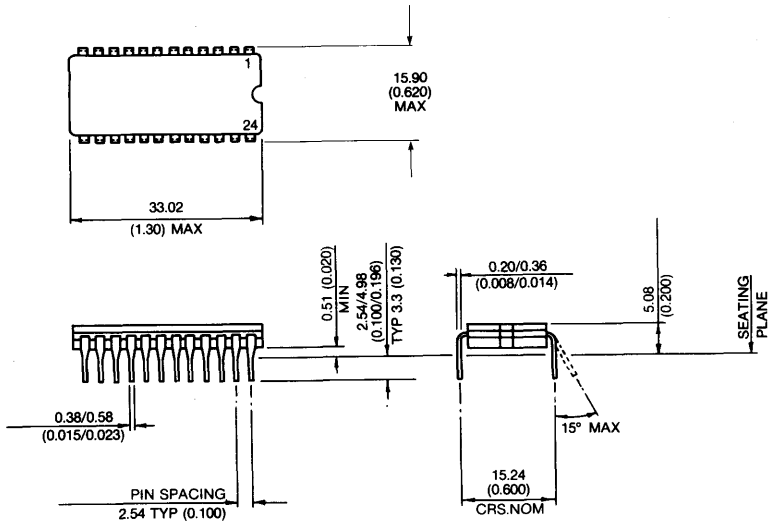
18 LEAD CERAMIC DIL
CERDIP - DG18

DG18



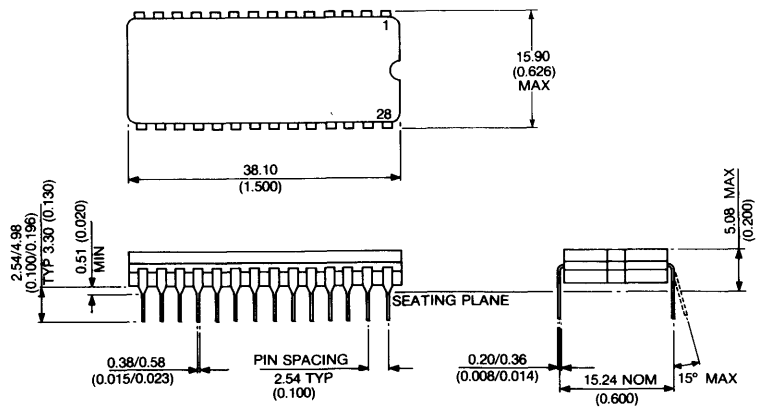
20 LEAD CERAMIC DIL
CERDIP - DG20

DG20



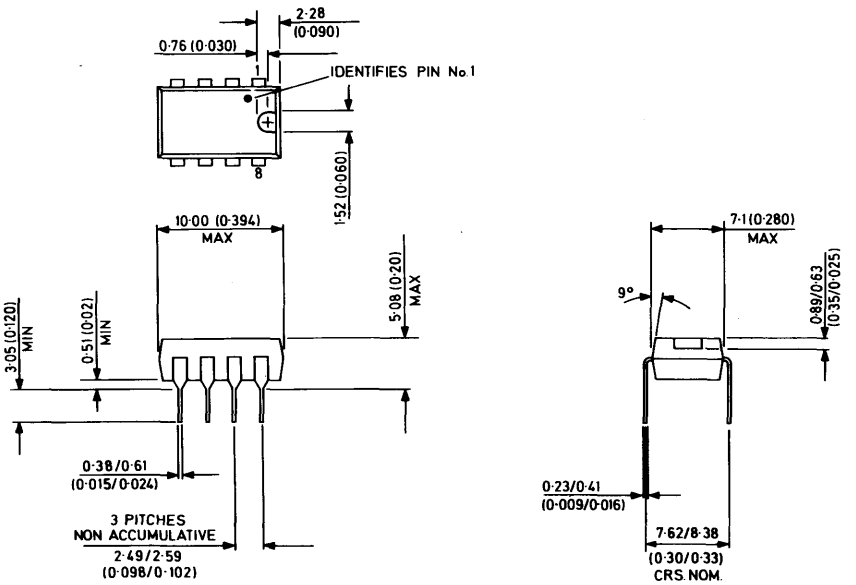
24 LEAD CERAMIC DIL
CERDIP - DG24

DG24

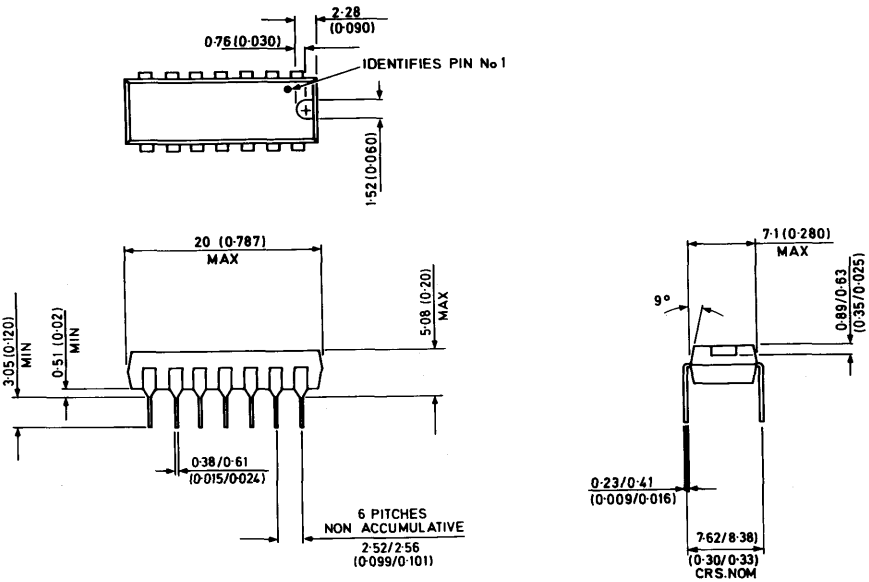


28 LEAD CERAMIC DIL
CERDIP - DG28

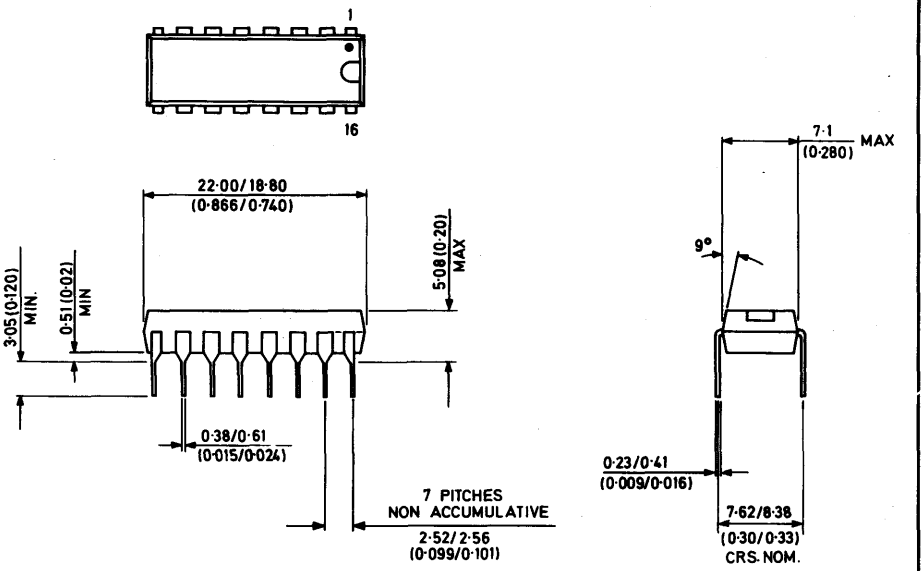
DG28



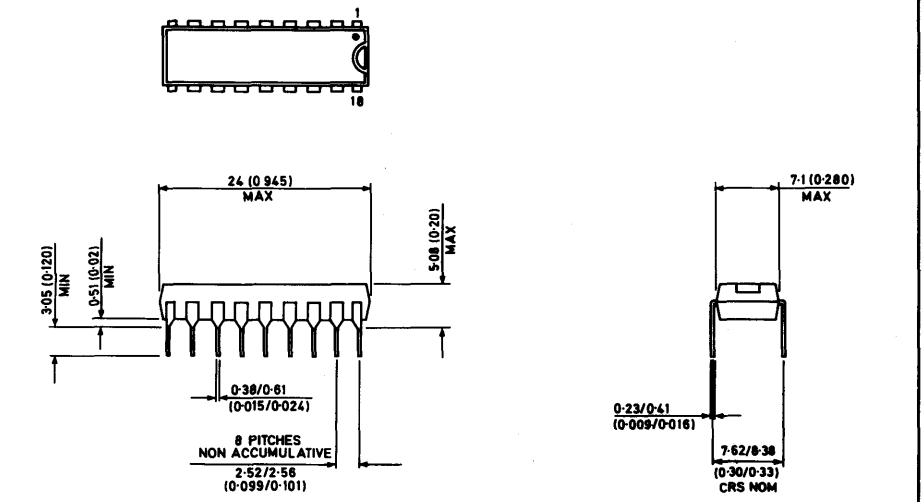
8 LEAD PLASTIC DIL **DP8**



14 LEAD PLASTIC DIL **DP14**



16 LEAD PLASTIC DIL **DP16**



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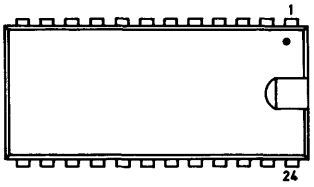

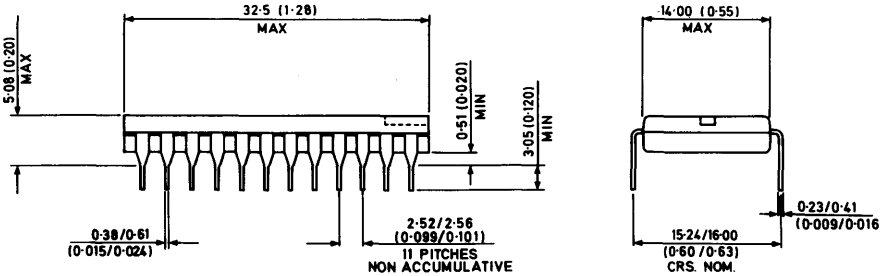

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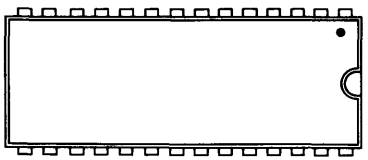
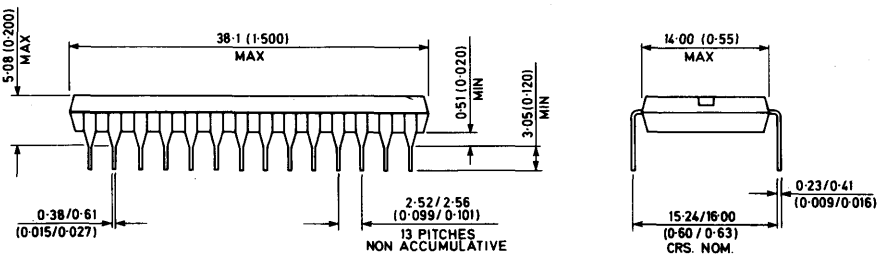
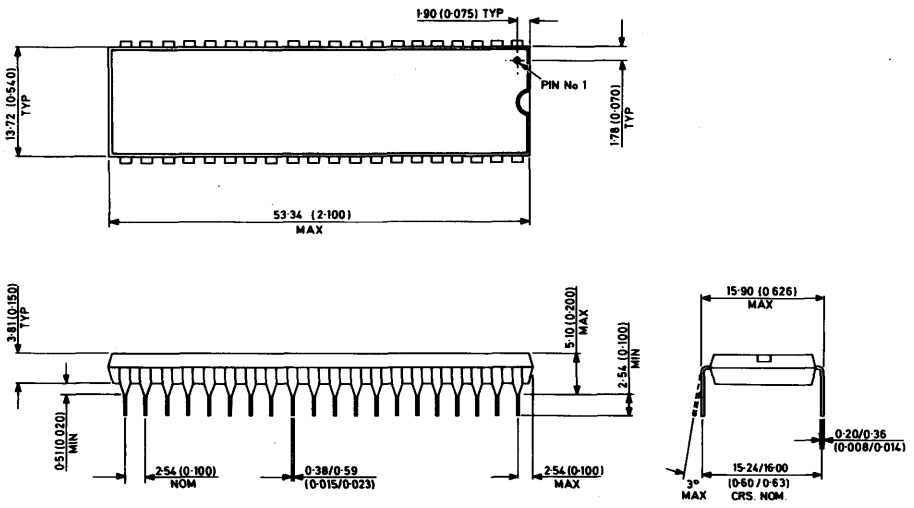




28 LEAD PLASTIC DIL **DP28**



40 LEAD PLASTIC DIL **DP40**

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